DIGCOM-A1.2 FPGA 실습키트

(VHDL, Verilog)

Quartus Prime Lite 21.1

2022년 3월 26일

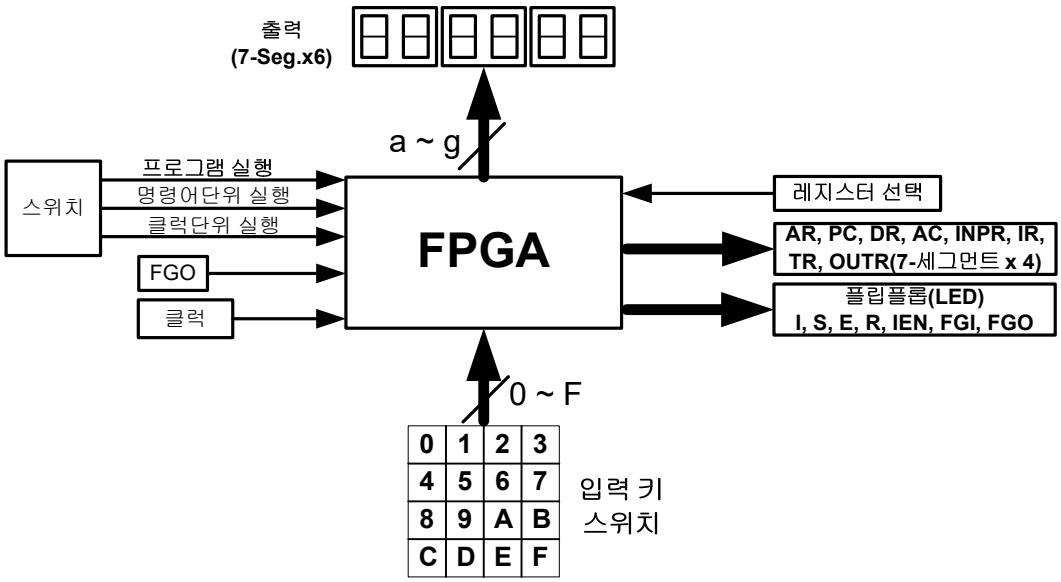
주식회사 인트모션

목 차

1. DIGCOM-A1.2 소개

1.1 DIGCOM-A1.2 개요

DIGCOM-A1.2 [1] . DIGCOM-A1.2
3 2 7- FND(Flexible
Numeric Display), 16 , 8 15
LED DIGCOM-A1.2 16
3 2 7-
FND 2 , 4
7 LED .
, .



DIGCOM-A1.2
,
. 2 FND 8 ,
0x0 ~ 0xF 16 16
. 8 .

2 7- FND
. LED . [

2] DIGCOM-A1.2

. DIGCOM-A1.2 FPGA

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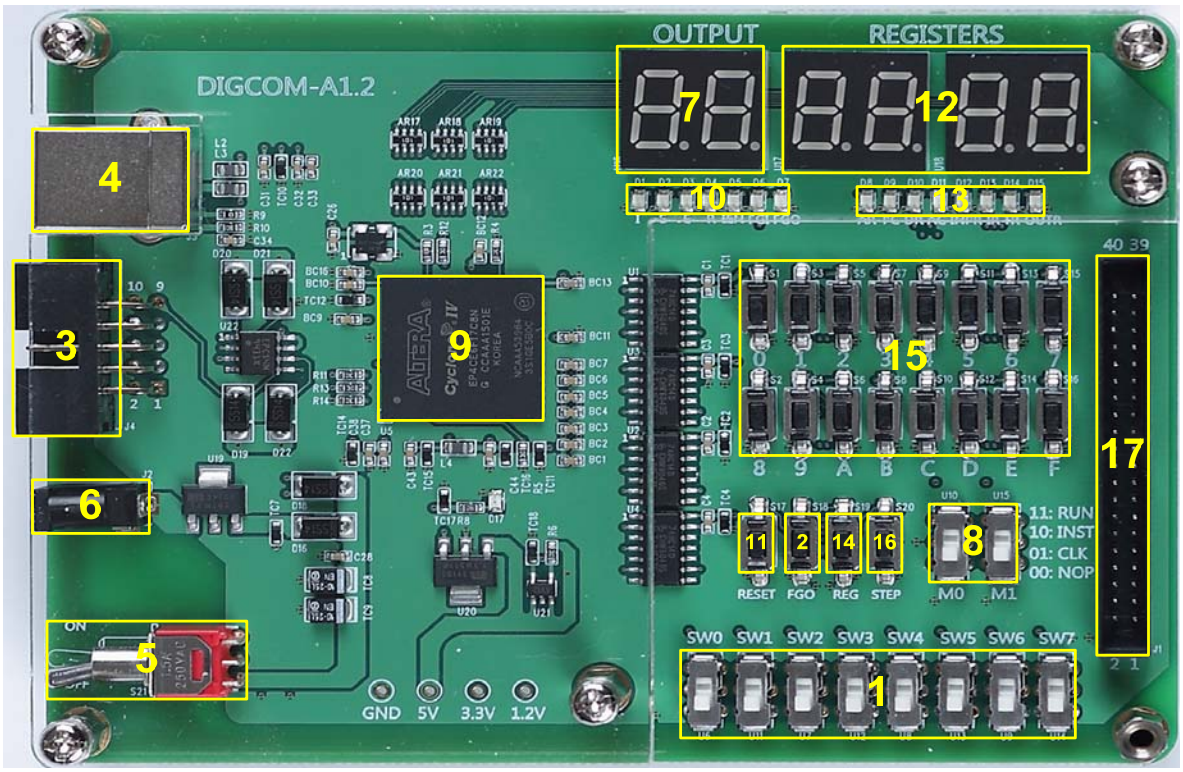

: ‘0’ ‘1’ .

8

FGO_SET : 7-

(FGO) “1”

.

USB Blaster : Active Serial EPCS4 configuration

. Configuration

.

CycloneIV FPGA .

USB : USB ,

USB .

: ON/OFF

: USB

.

2 7- FND : OUTR(Output Register)

.

: (run) ,

EP4CE6F17C8 CycloneIV FPGA : Verilgo VHDL “

” .

LED : 7 .

: .

7- FND : 8

.

LED .

LED : FND 8

.

:

FND .

: “0” “F” 16 .

16 : .

,

.

17 : FPGA DIGCOM-A1.2

.

1.2 DIGCOM-A1.2 설치

a. 전원연결

USB . USB

USB

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USB .

b. USB Blaster 다운로드 케이블 연결

USB USB USB Blaster USB ,
10 IDC USB Blaster JTAG DIGCOM-A1.2
USB Blaster .

2. Quartus Prime Lite 소프트웨어 설치

a. Intel 회원 가입

- 2015 Altera Intel Intel
.
- Intel
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b. 설계 소프트웨어 다운로드

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-
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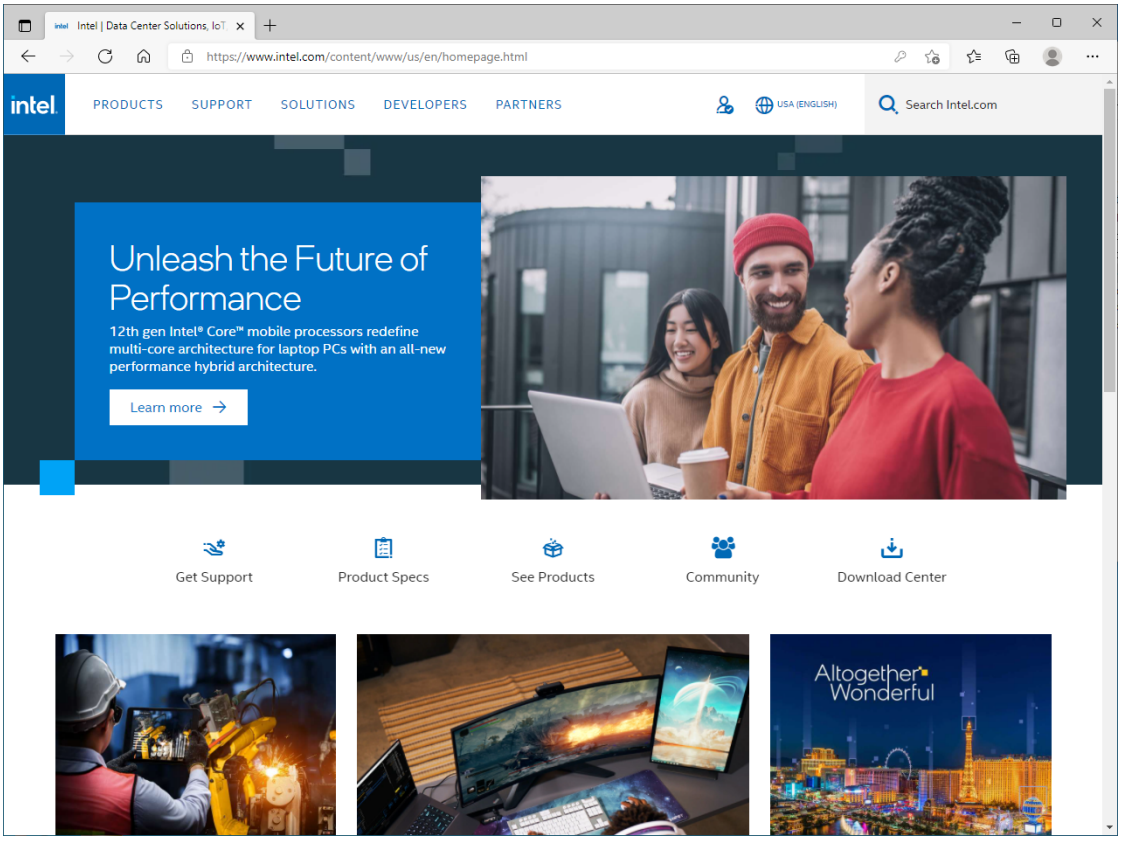
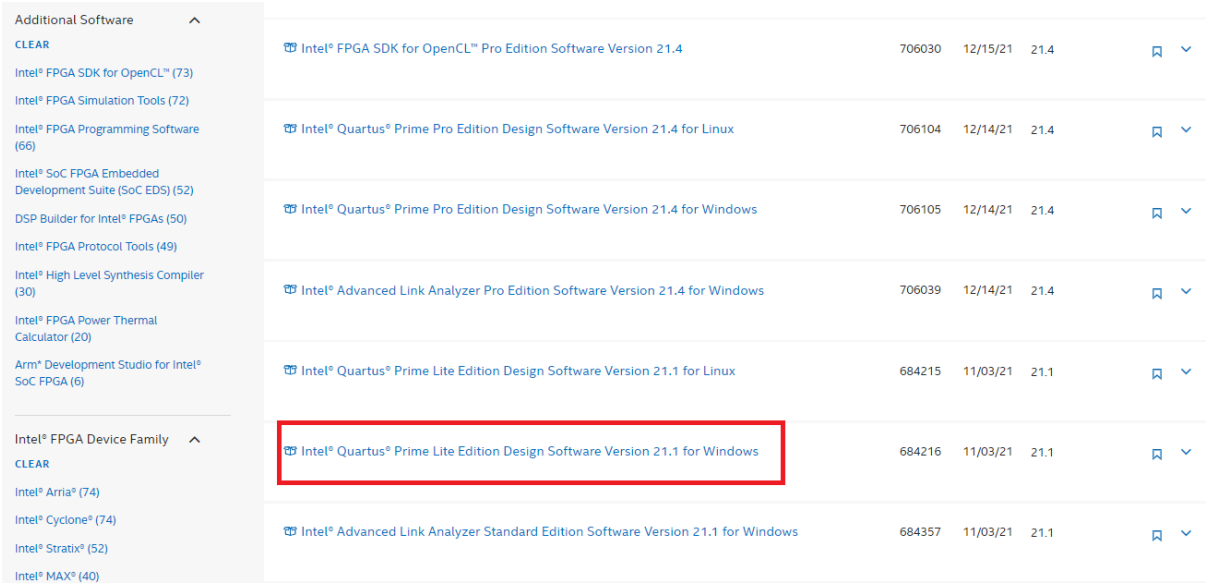
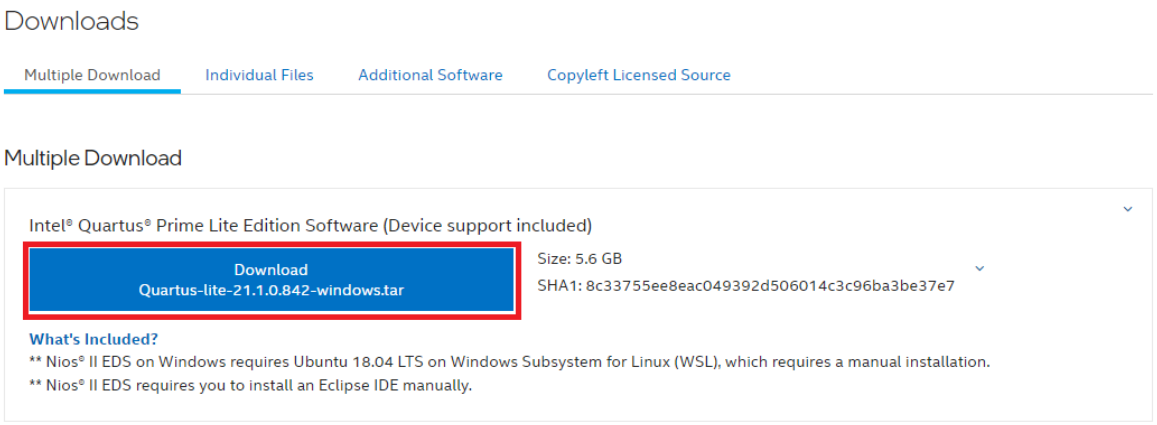


- , “Download Center Intel®” .



- “Intel® Quartus® Prime Lite Edition Design Software Version 21.1 for Windows”



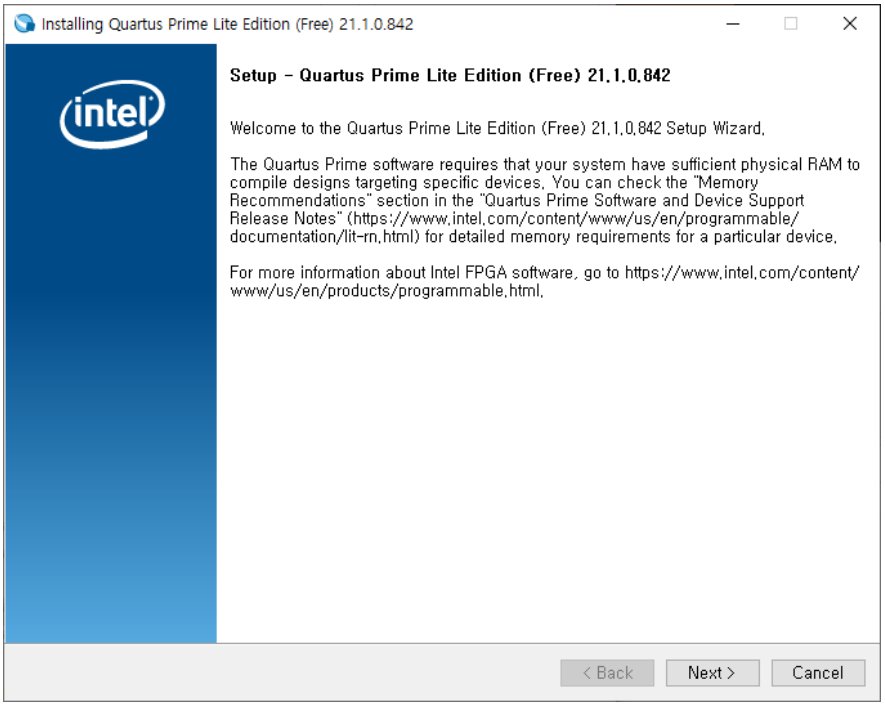
- ‘Download” “Software License Agreement”

.

c. 프로그램 설치

- “setup.bat”

, license .



- “Cyclone IV” ,

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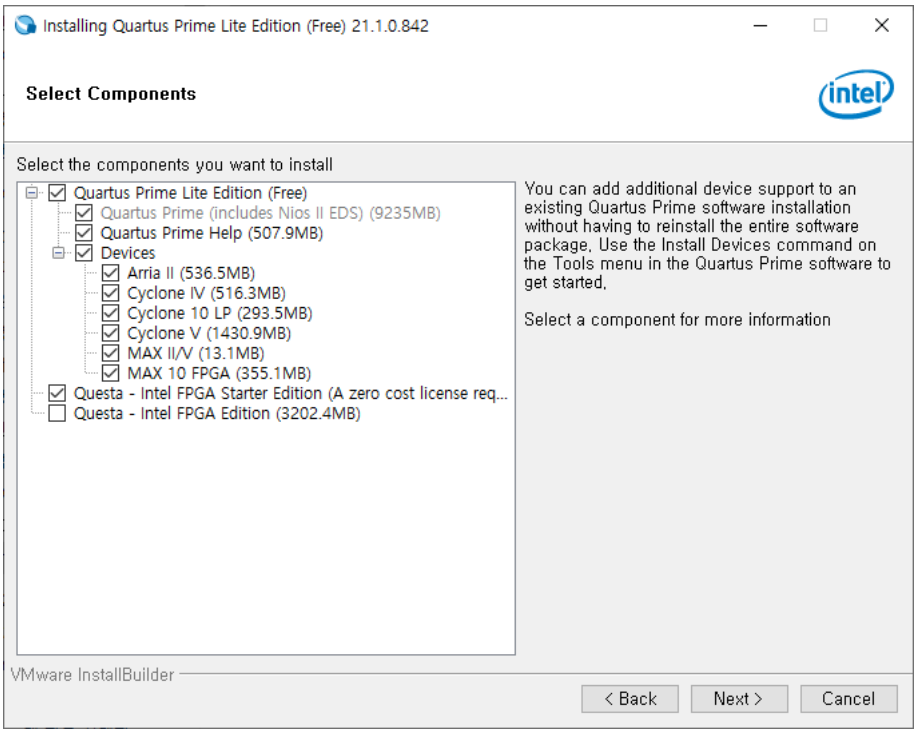
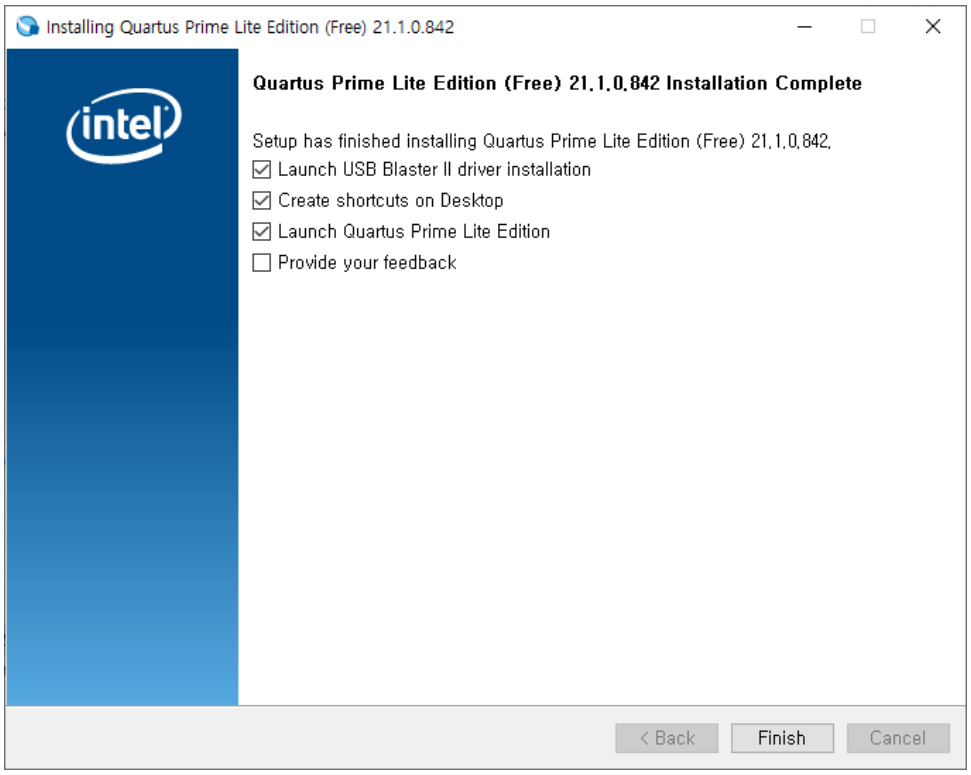
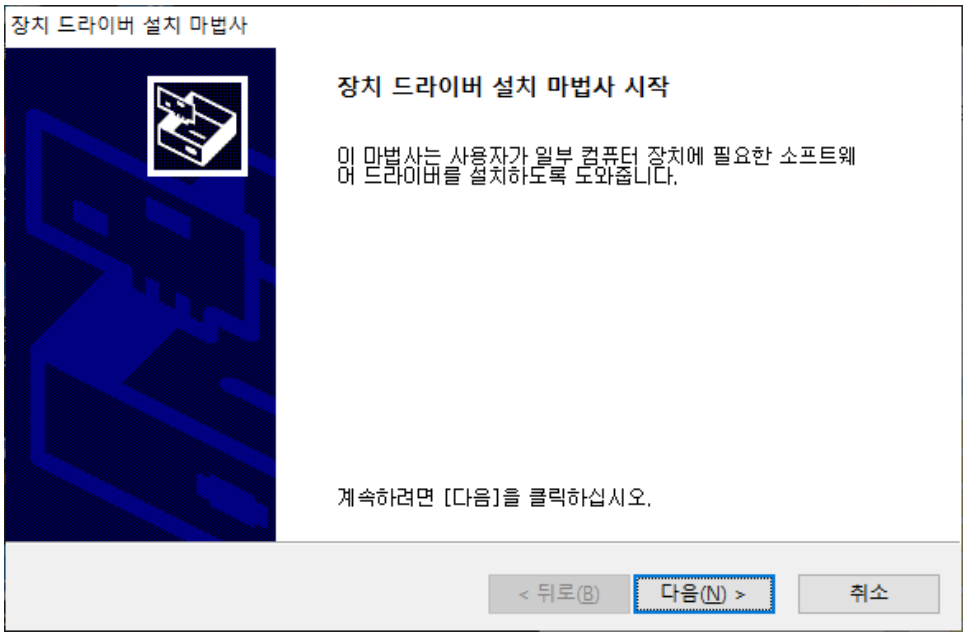
- “Questa-Intel FPGA Starter Edition”

.


Installing Quartus Prime Lite Edition (Free) 21.1.0.842
Select Components
Select the components you want to install
Quartus Prime Lite Edition (Free)
Quartus Prime (includes Nios II EDS) (9235MB)
Quartus Prime Help (507.9MB)
Devices
Arria II (536.5MB)
Cyclone IV (516.3MB)
Cyclone 10 LP (293.5MB)
Cyclone V (1430.9MB)
MAX II/V (13.1MB)
MAX 10 FPGA (355.1MB)
Questa - Intel FPGA Starter Edition (A zero cost license req...
Questa - Intel FPGA Edition (3202.4MB)
You can add additional device support to an existing Quartus Prime software installation without having to reinstall the entire software package. Use the Install Devices command on the Tools menu in the Quartus Prime software to get started.
Select a component for more information
VMware InstallBuilder
< Back
Next >
Cancel

-


Installing Quartus Prime Lite Edition (Free) 21.1.0.842
Quartus Prime Lite Edition (Free) 21.1.0.842 Installation Complete
Setup has finished installing Quartus Prime Lite Edition (Free) 21.1.0.842.
Launch USB Blaster II driver installation
Create shortcuts on Desktop
Launch Quartus Prime Lite Edition
Provide your feedback
< Back
Finish
Cancel


장치 드라이버 설치 마법사
장치 드라이버 설치 마법사 시작
이 마법사는 사용자가 일부 컴퓨터 장치에 필요한 소프트웨어 드라이버를 설치하도록 도와줍니다.
계속하려면 [다음]을 클릭하십시오.
< 뒤로(B)
다음(N) >
취소

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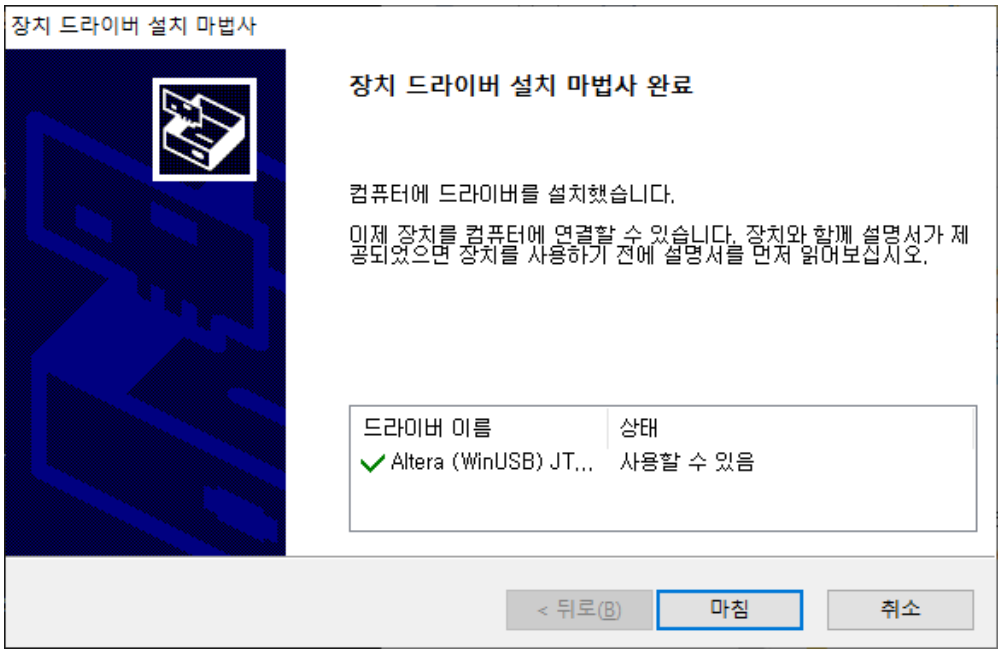
장치 드라이버 설치 마법사
장치 드라이버 설치 마법사 완료
컴퓨터에 드라이버를 설치했습니다.
이제 장치를 컴퓨터에 연결할 수 있습니다. 장치와 함께 설명서가 제공되었으면 장치를 사용하기 전에 설명서를 먼저 읽어보십시오.
드라이버 이름
상태
Altera (WinUSB) JT...
사용할 수 있음
< 뒤로(B)
마침
취소

3. Questa Simulator를 사용하기 위한 라이선스 설치

a. 설치할 컴퓨터의 네트워크 카드 물리적 주소 찾기

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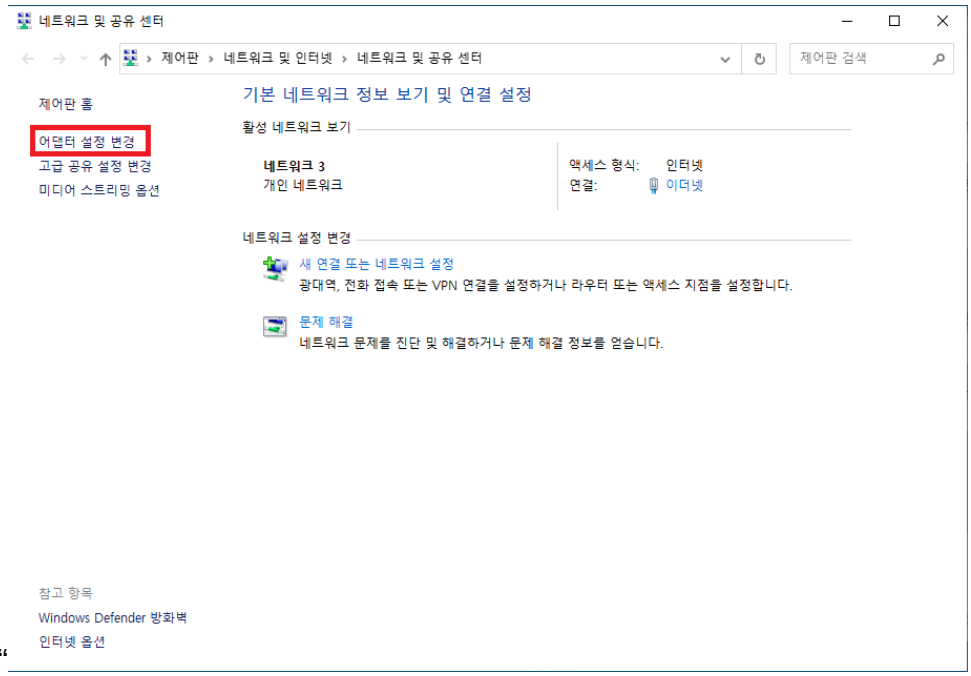

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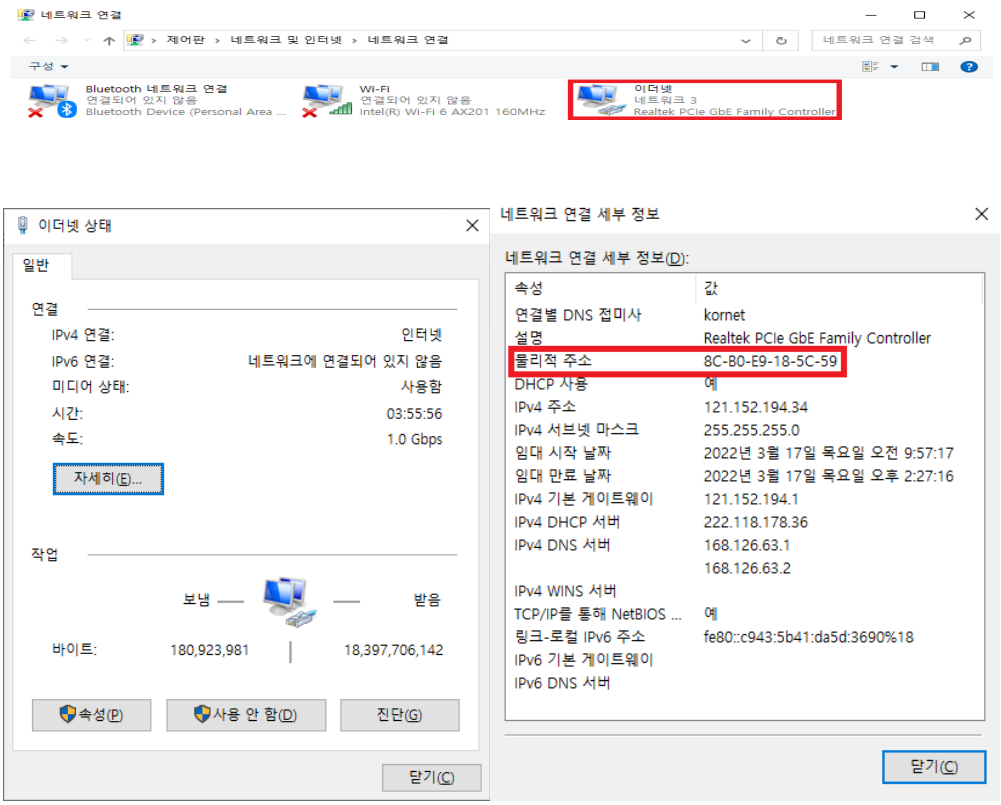
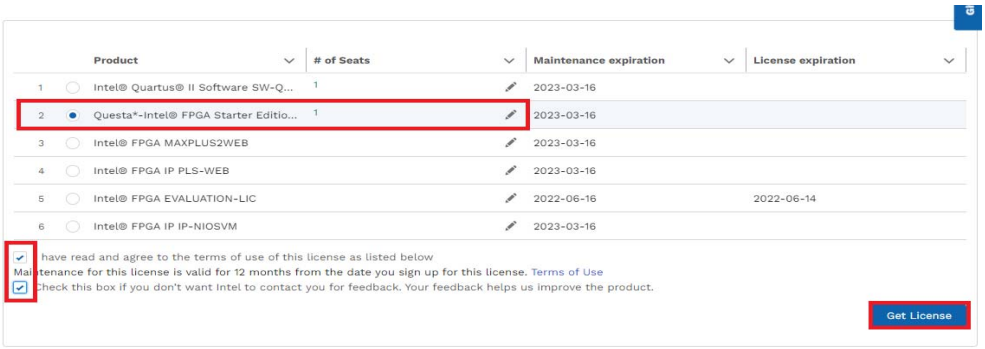


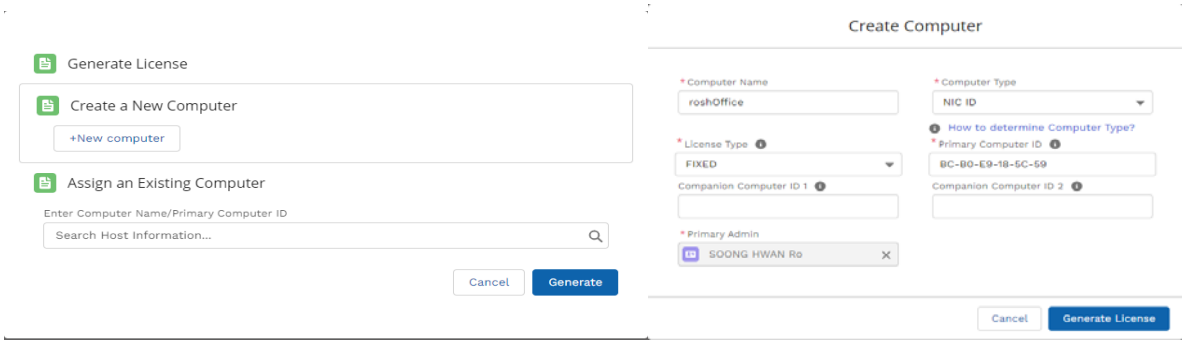
b. 라이선스 받기

- Intel **“Intel® FPGA Self-Service Licensing Center”** .
- URL https://licensing.intel.com/psg/s/sales-signup-evaluationlicenses” .
- “Questa*-Intel® FPGA Starter Edition” , “# of Seats” 1 , ( ) “Get License” .



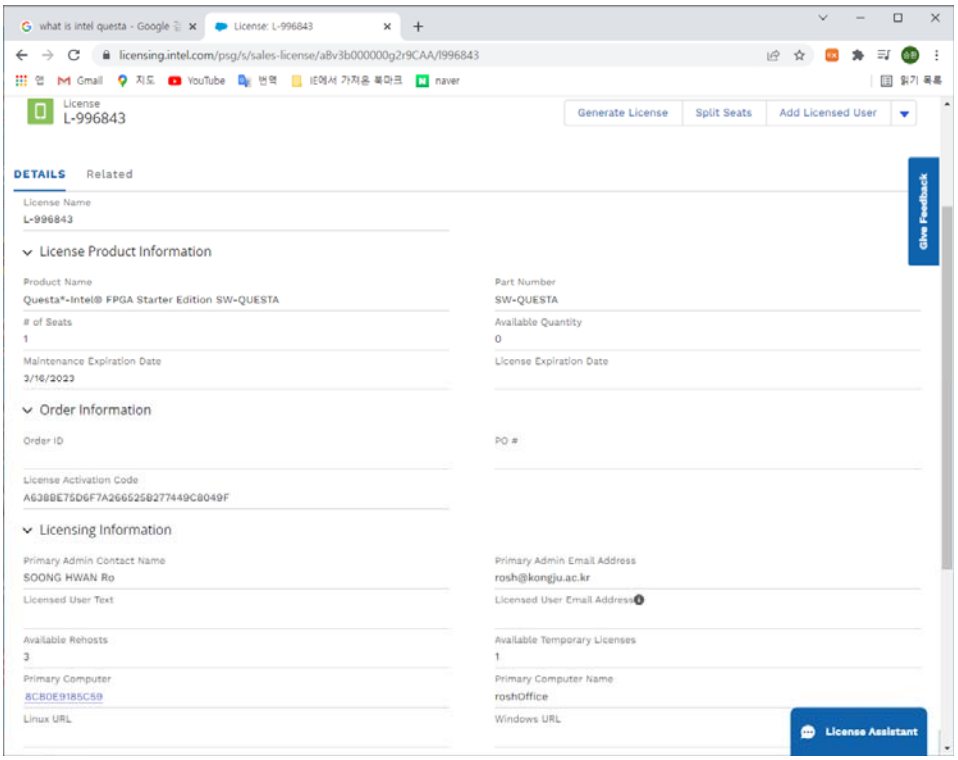
- “Questa*-Intel® FPGA Starter Edition” , “# of Seats” 1 , ( ) “Get License”
.

- “Create a New Computer” . “Assign an Existing Computer” “Generate” , .



- “Questa*-Intel® FPGA Starter Edition” , “# of Seats” 1 , ( ) “Get License”
, .

- (LR-074286_License.dat) Quartus . (C: \ intelFPGA_lite \ 21.1 \ licenses \ LR-074286_License.dat)



c. 컴퓨터에 라이선스 환경 설치하기(LM_LICENSE_FILE 환경 변수 설정)

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- “ ”

“ ”

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- “ ” “ ” .

- “ ” “ ” “ ”
“LM_LICENSE_FILE”, “ ”
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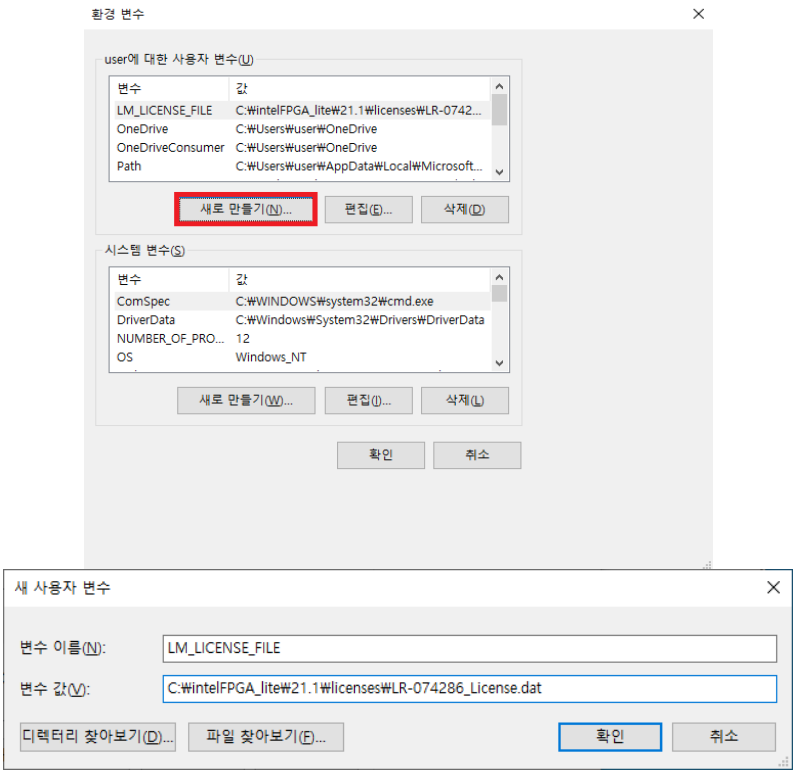


4. Quartus Prime Lite 소프트웨어 사용

Verilog VHDL Quartus Prime Lite Software

. ,

.

,

.

, ,

, FPGA configuration .

4.1 프로젝트 생성과 컴파일

a. 새 프로젝트 생성(Create a Project)과 코드 작성

- Verilog VHDL Quartus Prime Design Software

. ,

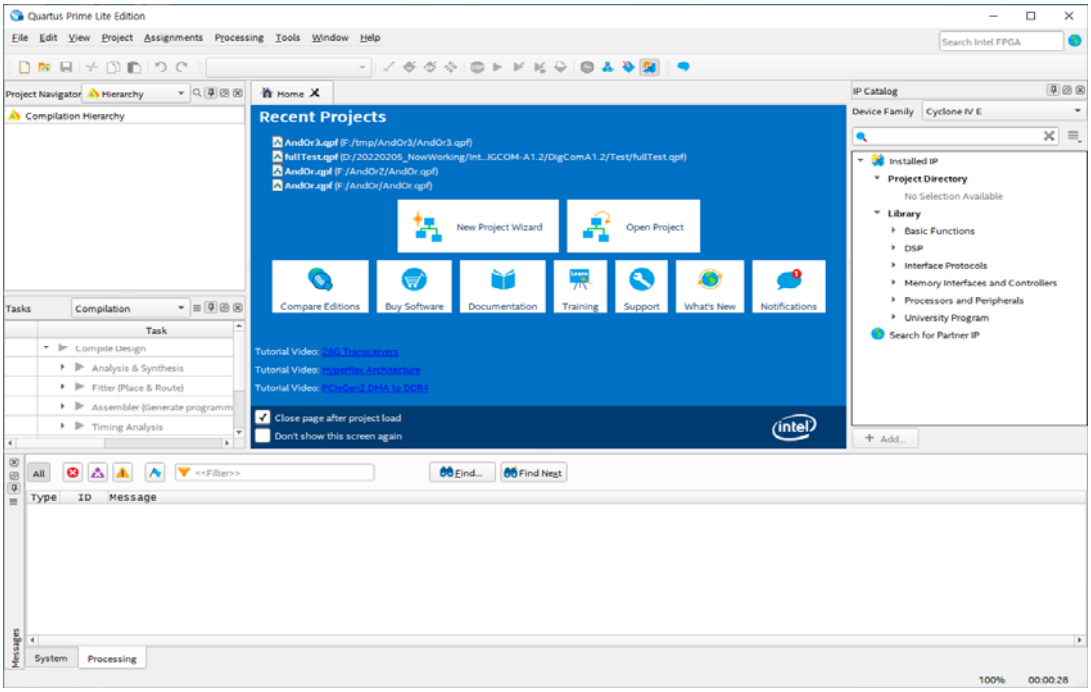
, , FPGA configuration

.

- Quartus Prime Lite Software ,

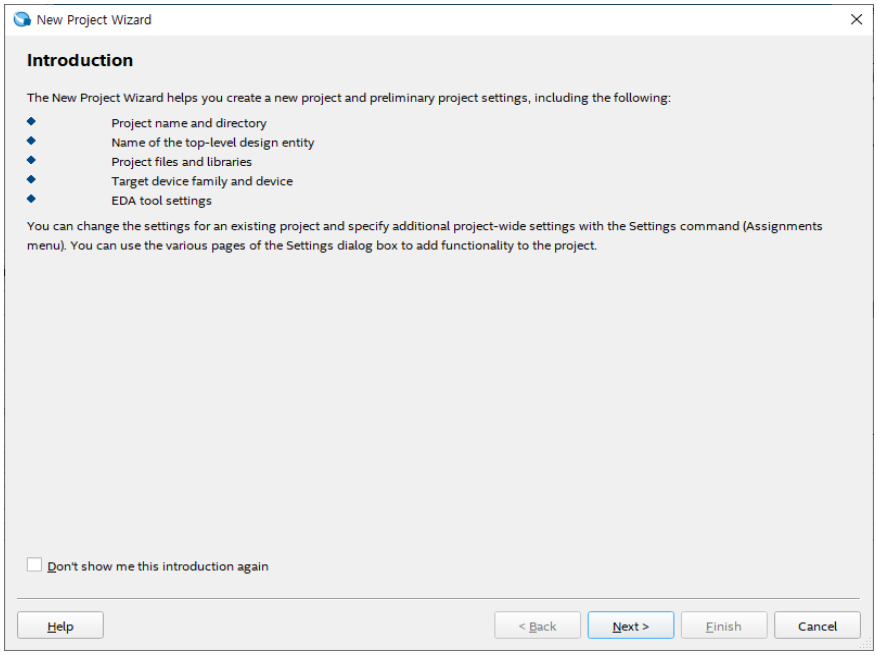
[File]-[New Project Wizard] Home

[New Project Wizard] .



- New Project .

[Next] .

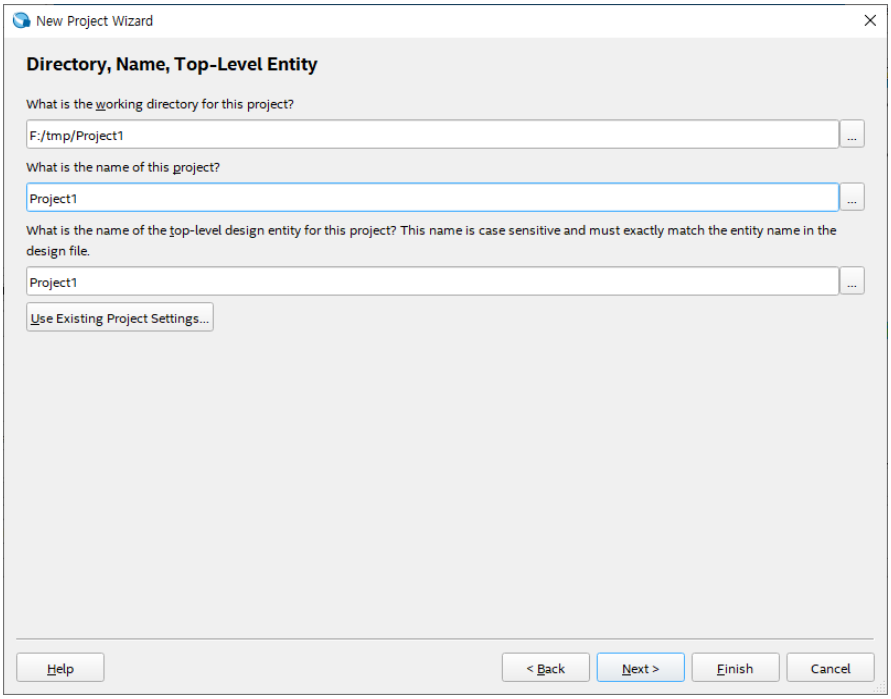


- Project Name .

,

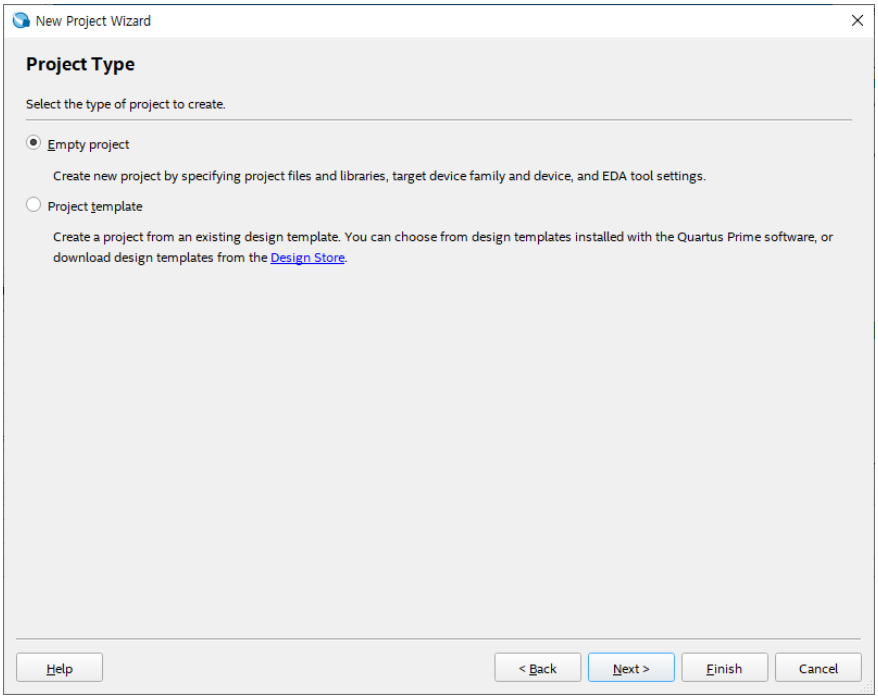
top-level design entry name .

[Next] .



- Project Type .

‘Empty project’ [Next] .

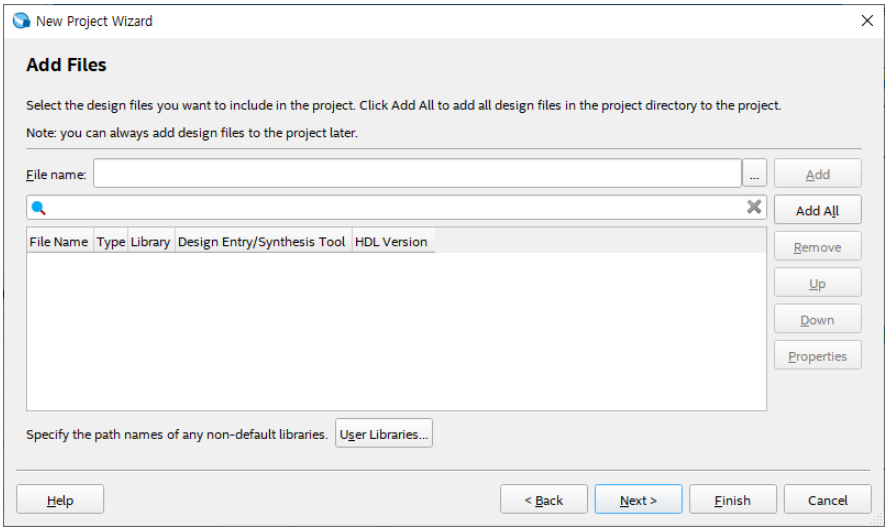


- .

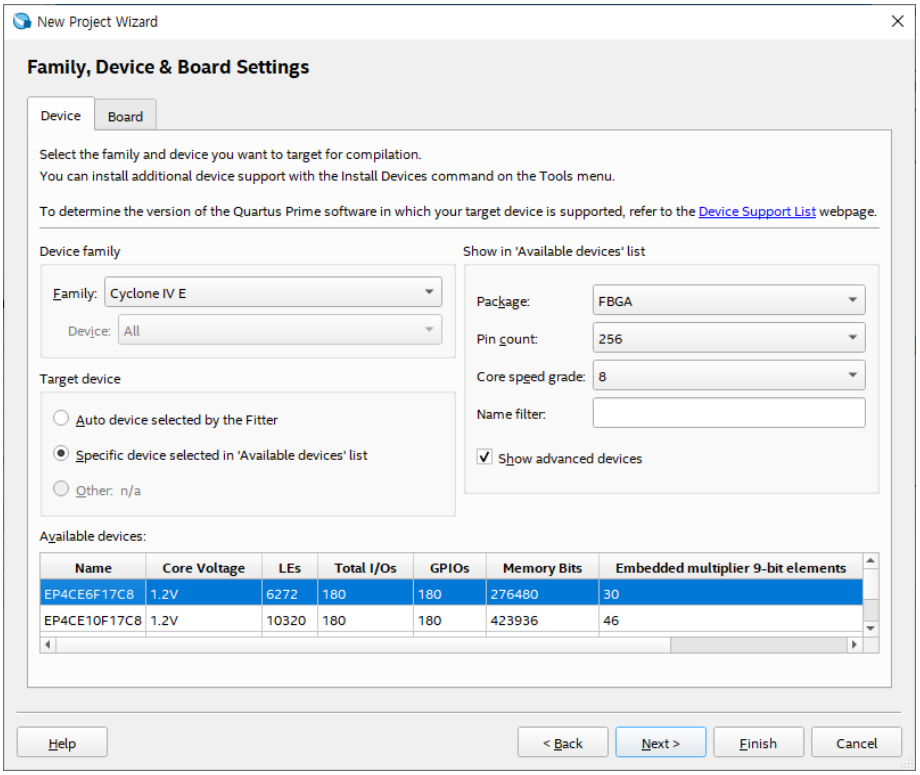
[Next] .

[Next]

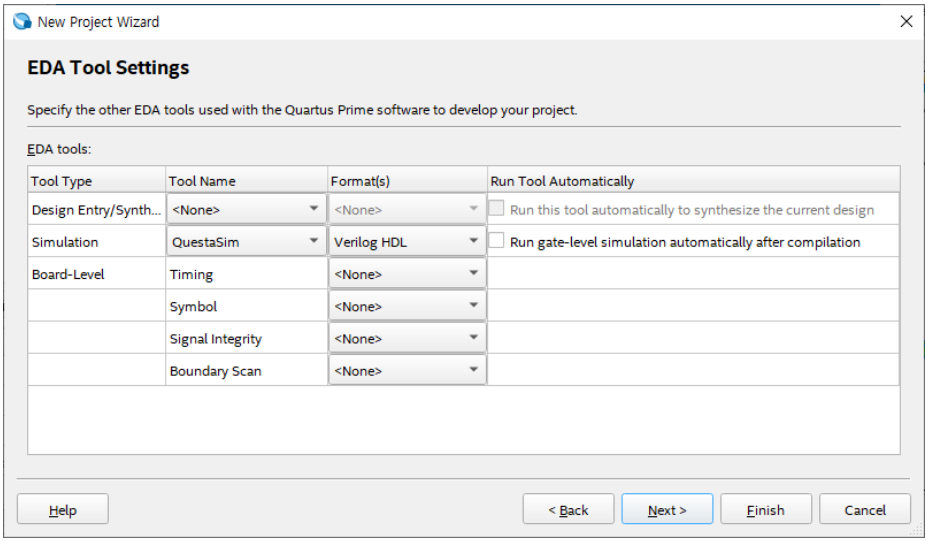
.



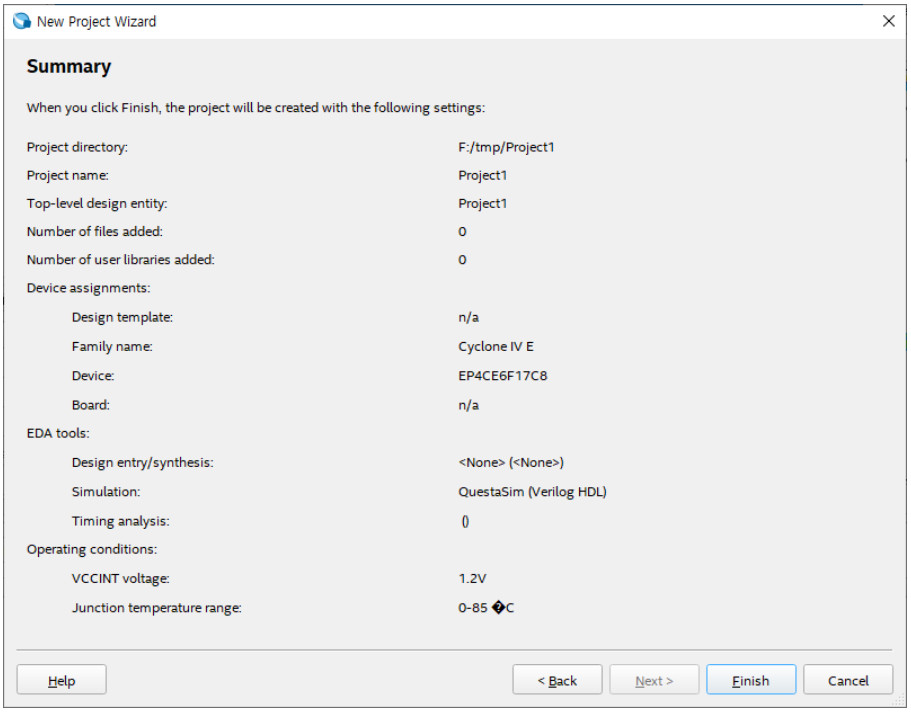
- . Family ‘Cyclone IV E’ , , Package ‘FBGA’, Pin count ‘256’, Core Speed grade ‘8’ . ‘EP4CE6F17C8’ [Next] .



- EDA Tool . “Tool Name” “QuestaSim”, “Format(s)” “Verilog HDL” .



- “Finish” .



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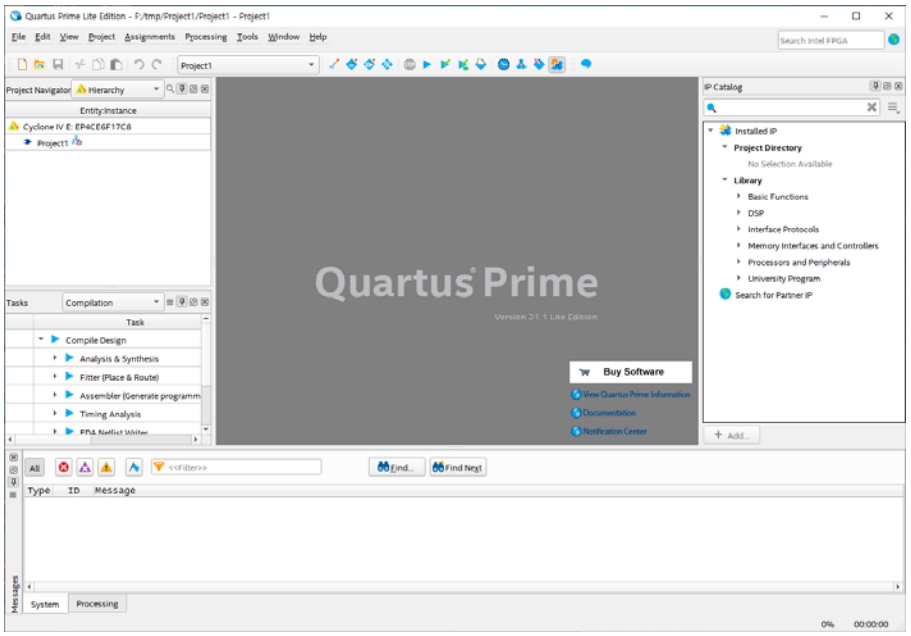


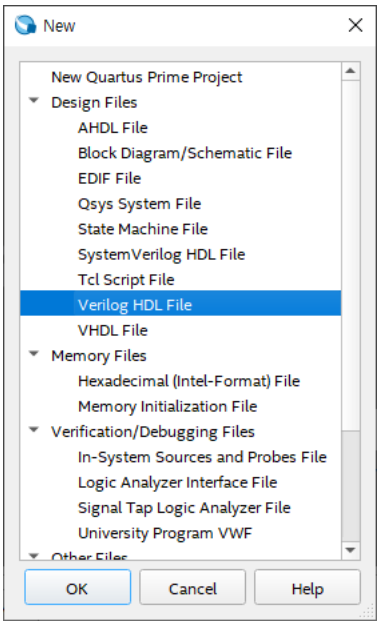
- Verilog VHDL . [File]-[New]

[New] .

. Verilog

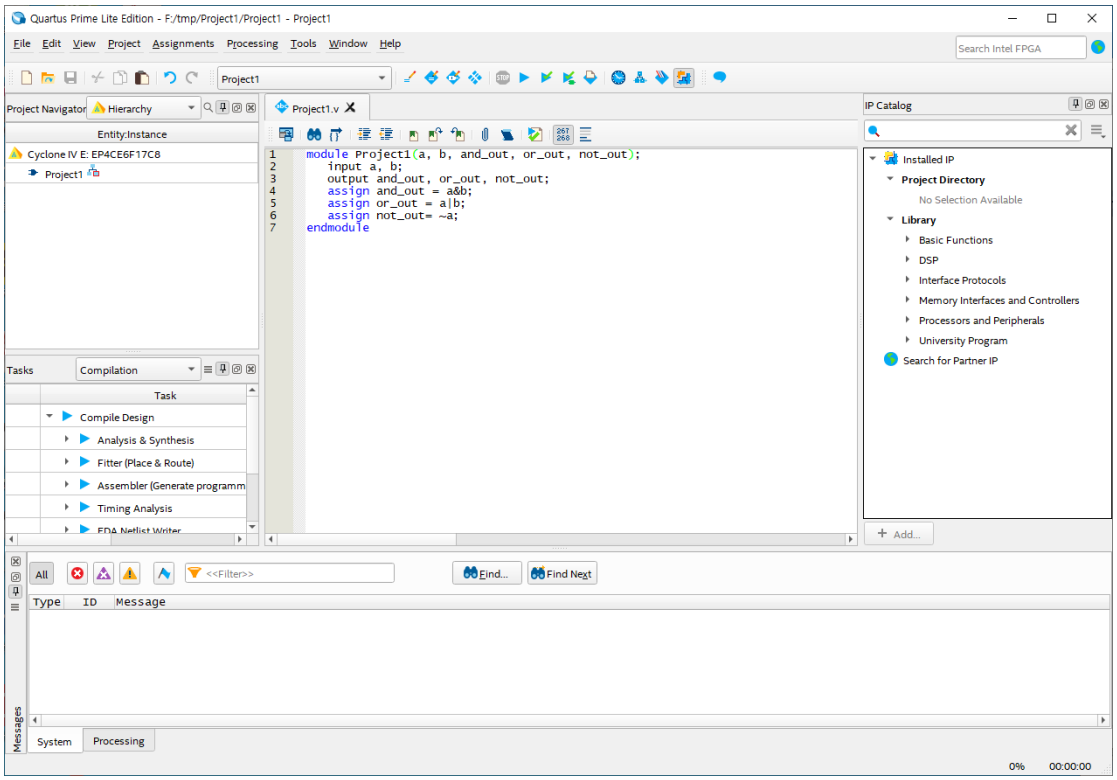
‘Verilog HDL File’ [OK] . VHDL

‘VHDL File’ [OK] .



- .

(Project1) .



-

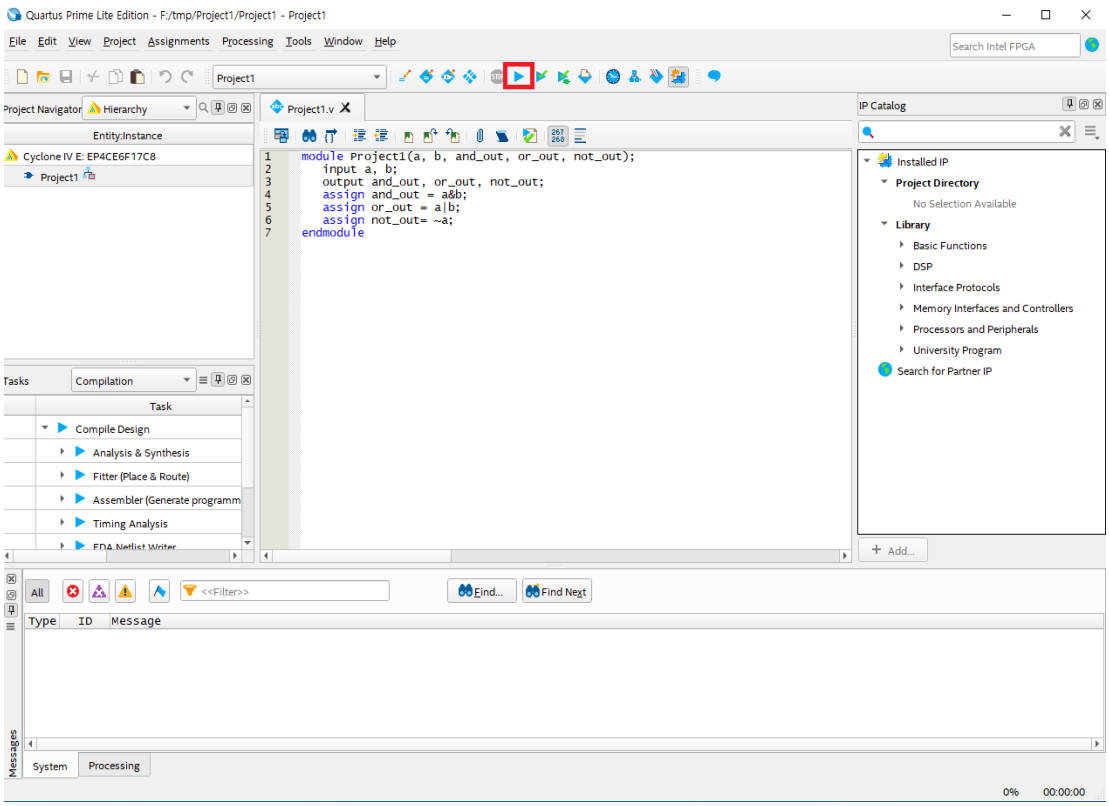
. Quartus Prime Design Software [File]-[Open Project] ,
(Project1.qpf)

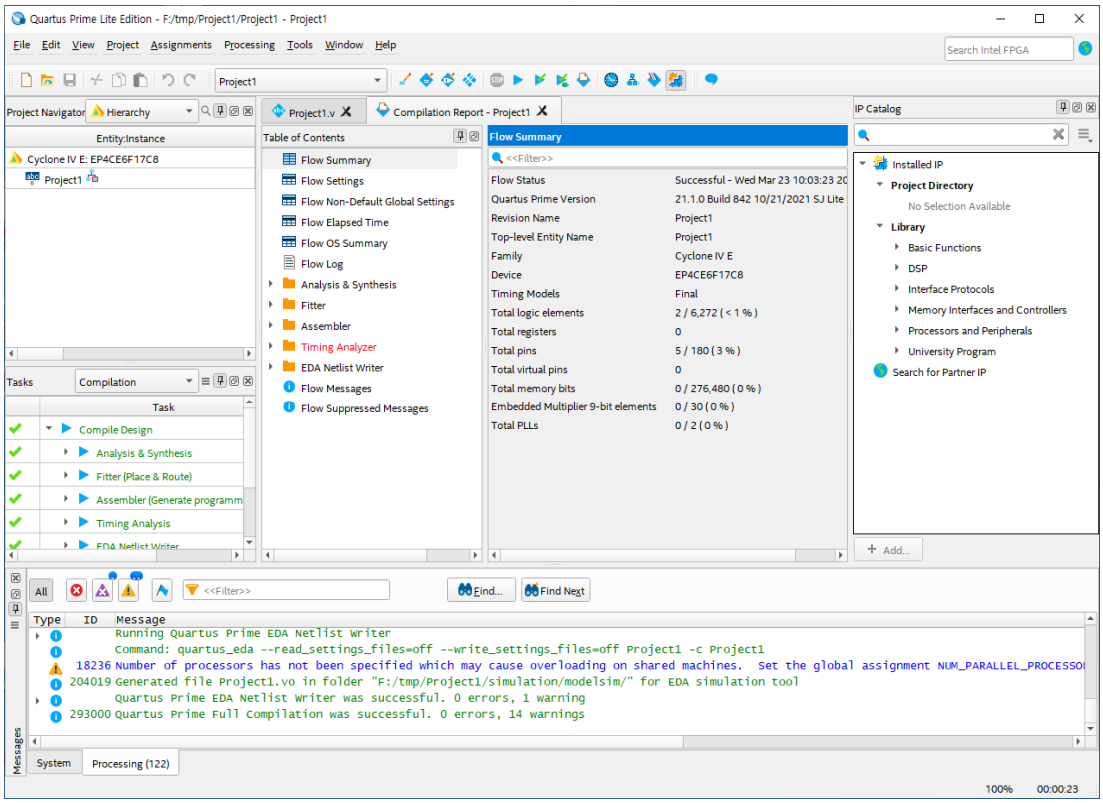
.

b. 코드(Verilog, VHDL) 컴파일(Compile)

- Synthesis . ,
Behavior RTL: Register Transfer Level Abstract Form Logic Gate . [Processing]-[Start Compilation]
[Start Compilation]

.





4.2 시뮬레이션

Simulation Verilog VHDL

. FPGA

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. FPGA

. Intel-Altera VWF(Vector Waveform Form)

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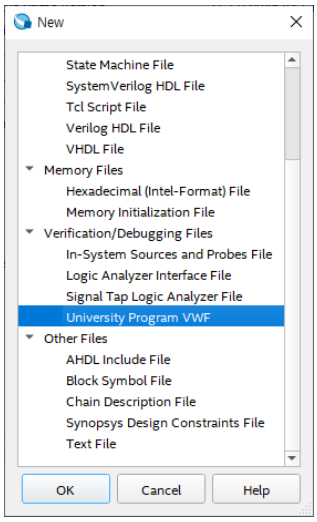
a. 시뮬레이션 입력 파형 지정

- [File]-[New]

. ‘University Program VWF’ [OK]

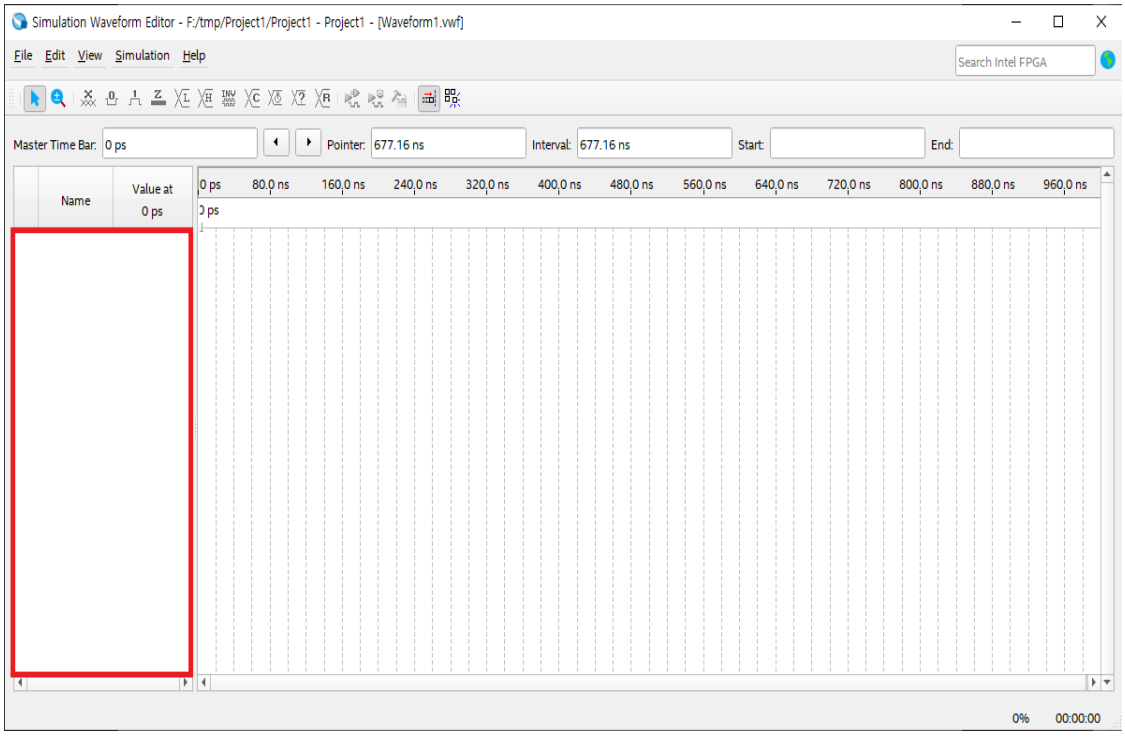


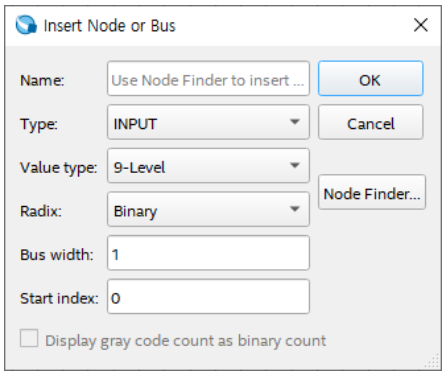
b. **입출력 포트 추가**

- Simulation Waveform Editor , VWF .

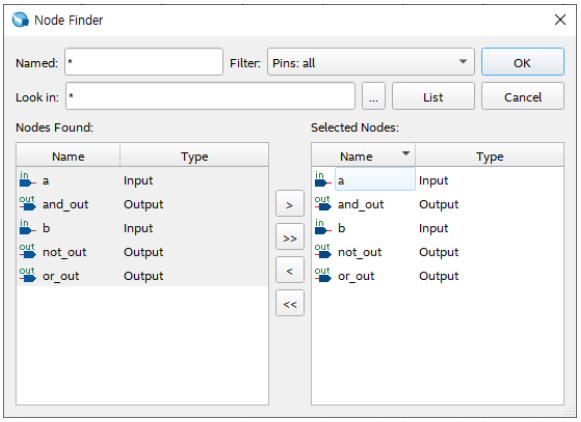
/

[Insert Node or Bus...] [Insert Node or Bus] .





- Insert Node or Bus [Node Finder...] Node Finder . Filter: Pins: all [List] Verilog VHDL . Nodes Found: “>>” Selected Nodes: [OK] . Insert Node or Bus [OK] .

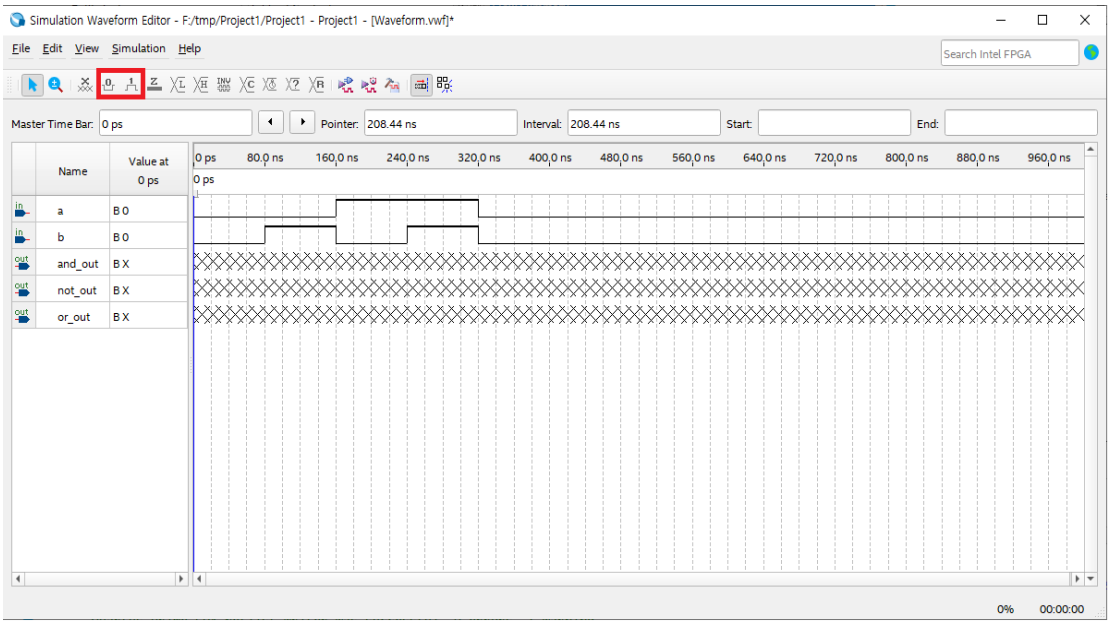


c. 입력 파형 지정

- .

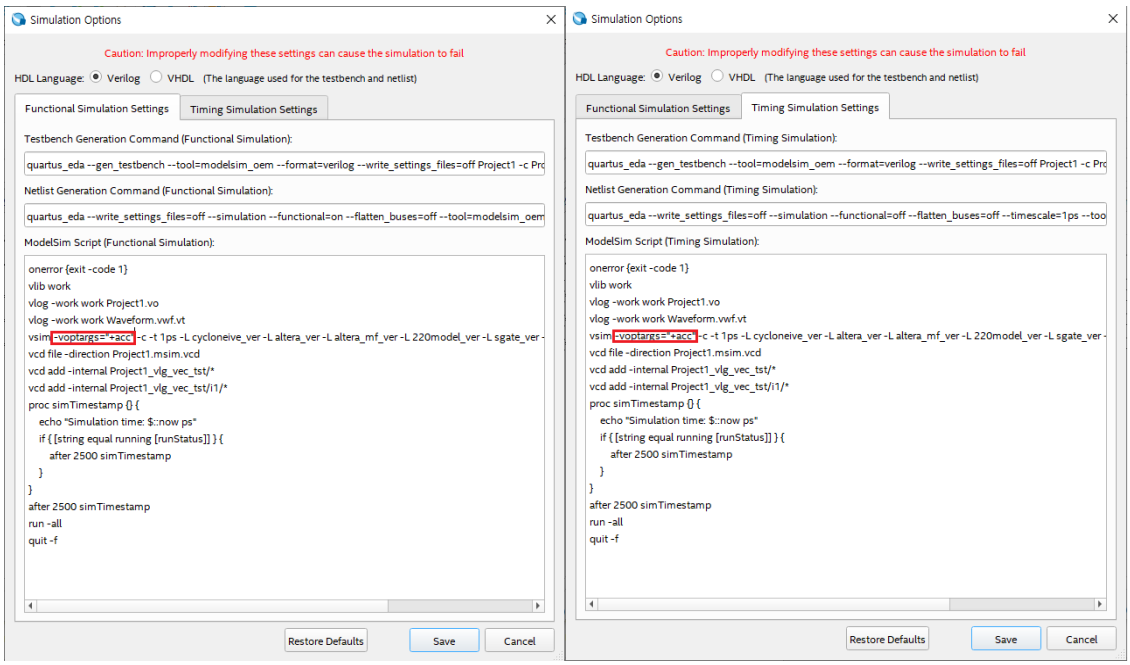
‘Waveform.vwf’ .

, .



d. 시뮬레이션 설정

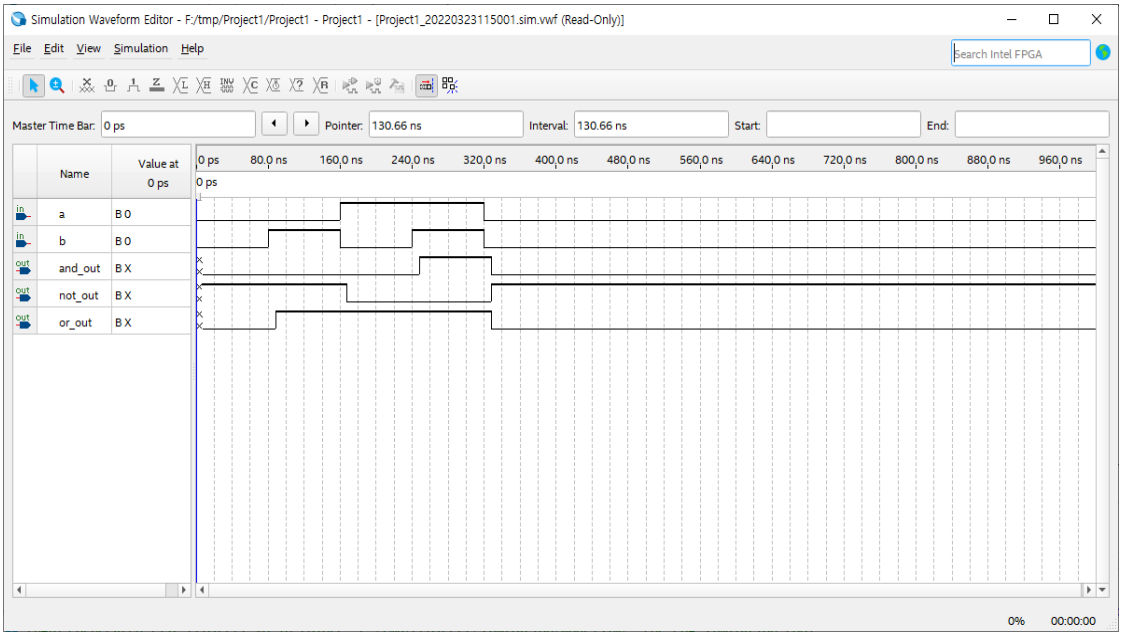
- [Simulation]=>[Simulation Settings] [Simulation Options] .
  [Functional Simulation Settings] [Timing Simulation Settings] [-novopt] [-voptargs=”+acc”] .



e. **시뮬레이션**

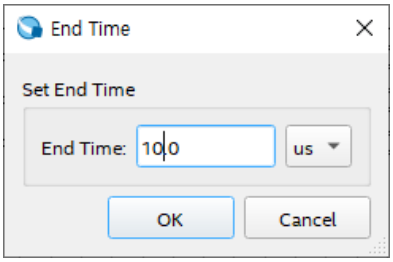
- Simulation Waveform Editor Simulation [Run Timing Simulation] [Run Functional Simulation] . [Functional Simulation] ,
  . [Timing Simulation]
  ,
  . Simulation Waveform Editor [Simulation]-[Run Timing Simulation]

.



f. **시뮬레이션 시간 변경**

- 1usec , [Edit]-[Set End Time]
  .



4.3 디바이스와 핀 할당(Device and Pin Assignment)

DIGCOM-A1.2 FPGA

. FPGA

.

a. 디바이스 종류 선택

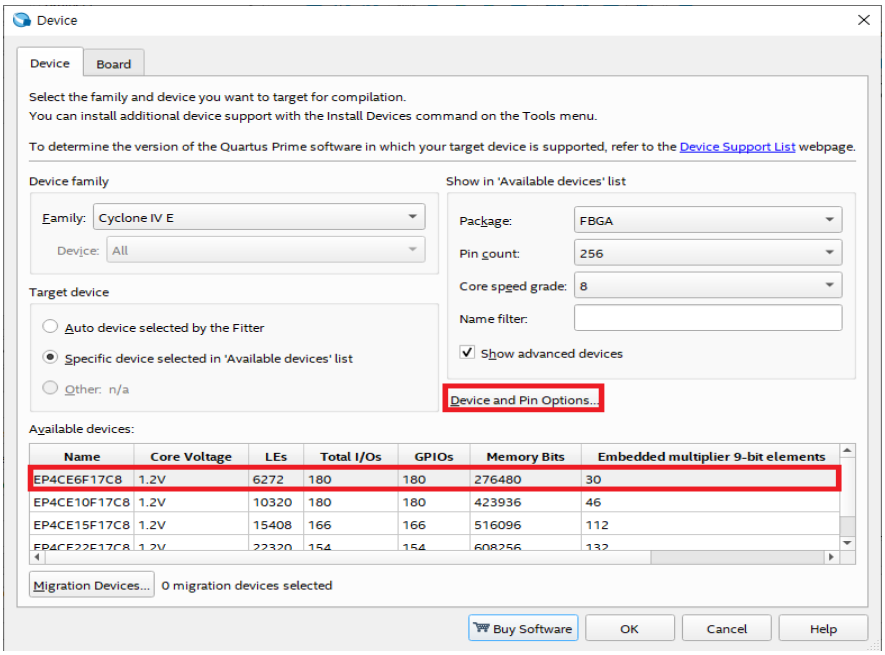
- DIGCOM-A1.2 Cyclone IV EP4CE6F17C8

  [Assignments] ➔ Device] Cyclone IV EP4CE6F17C8 .

  configuration device [Device and Pin Options...] . FPGA off

  , Configuration device

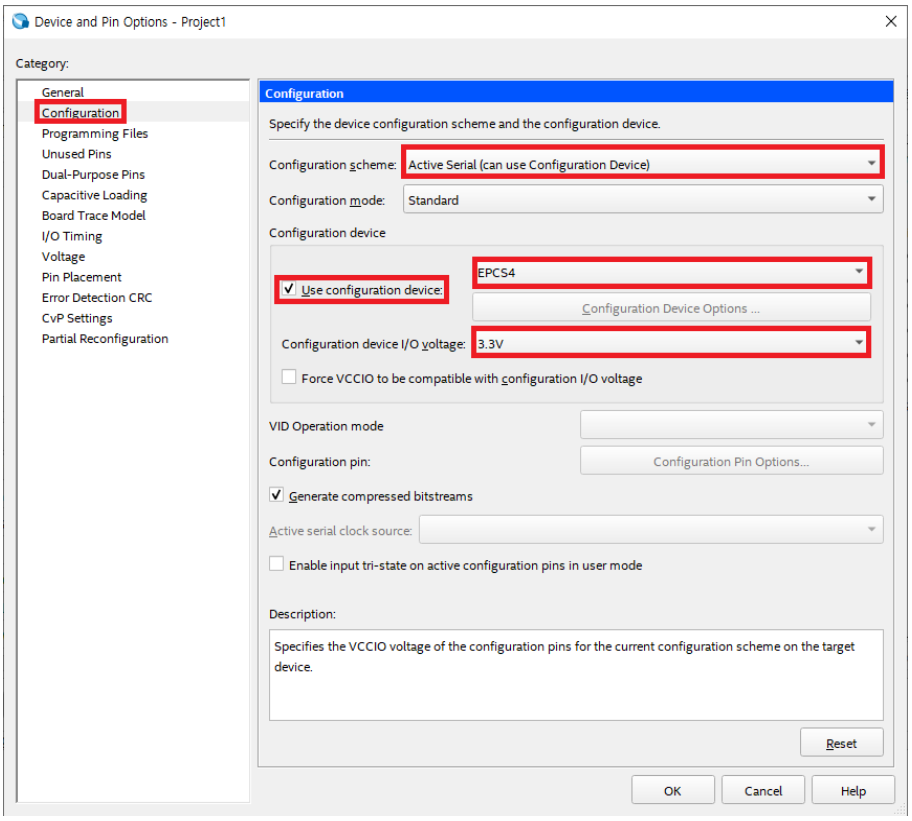
  .



b. 디바이스 옵션 설정

- Device and Pin Options . [Category] 'Configuration'

  Configuration scheme: 'Active Serial(can use Configuration Device)' . 'Use configuration device' configuration device 'EPCS4' , configuration device I/O voltage '3.3V' .



- Cyclone

. configuration EPCS4

. configuration ,

pof Programmable Object File .

,

Cyclone configure .

c. **사용하지 않는 핀 설정**

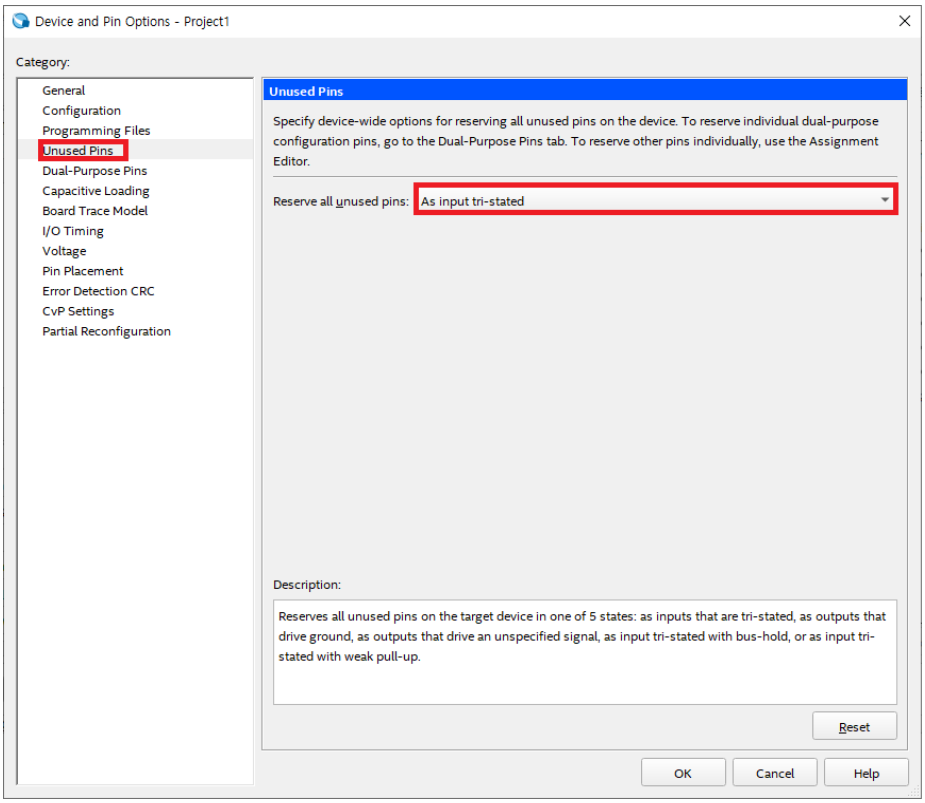
- Device and Pin Options Category: Unused Pins .

Reserve all unused pins: ‘As input tri-stated’ [OK]

. PGA

,

.



d. **디바이스 핀 할당**

- Cyclone IV ,

LED

.

.

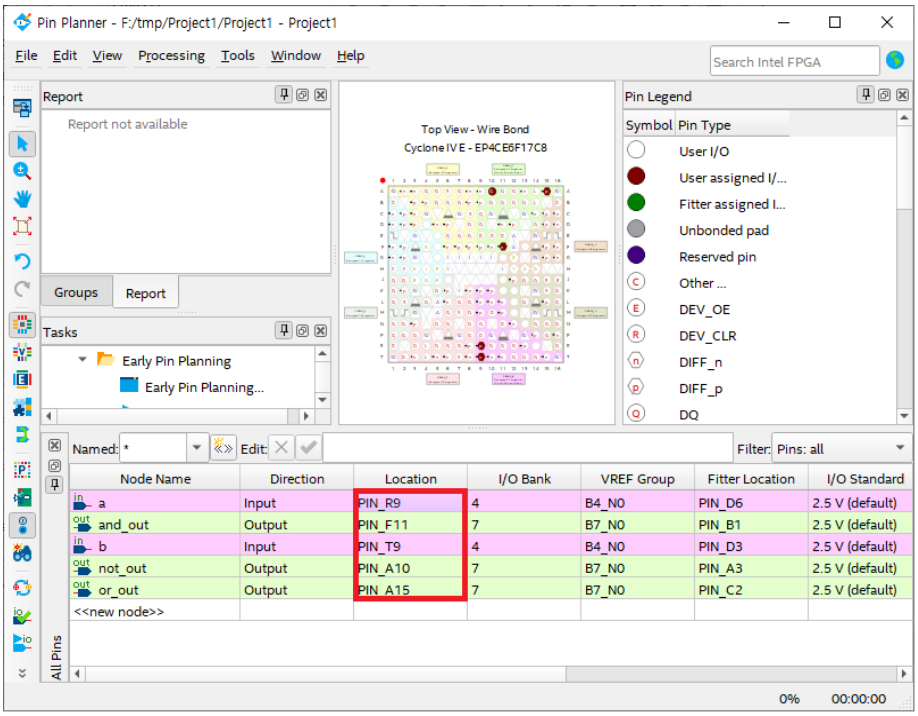
- Quartus Prime Lite Edition

[Assignment ➔ Pin Planner] Pin Planner .

. ,

.

.

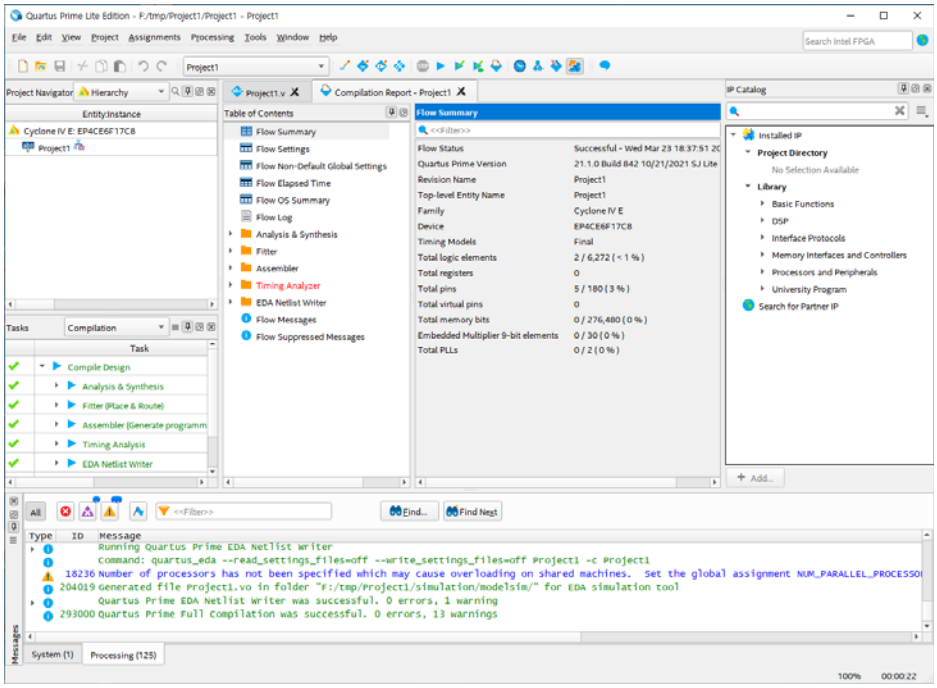


e. **컴파일**

- . pof

. pof

, configuration FPGA .

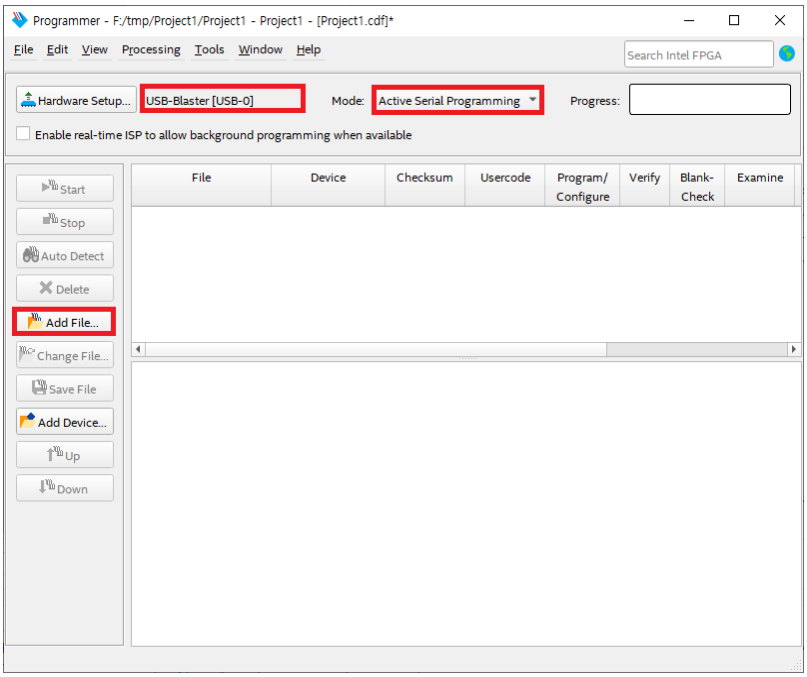


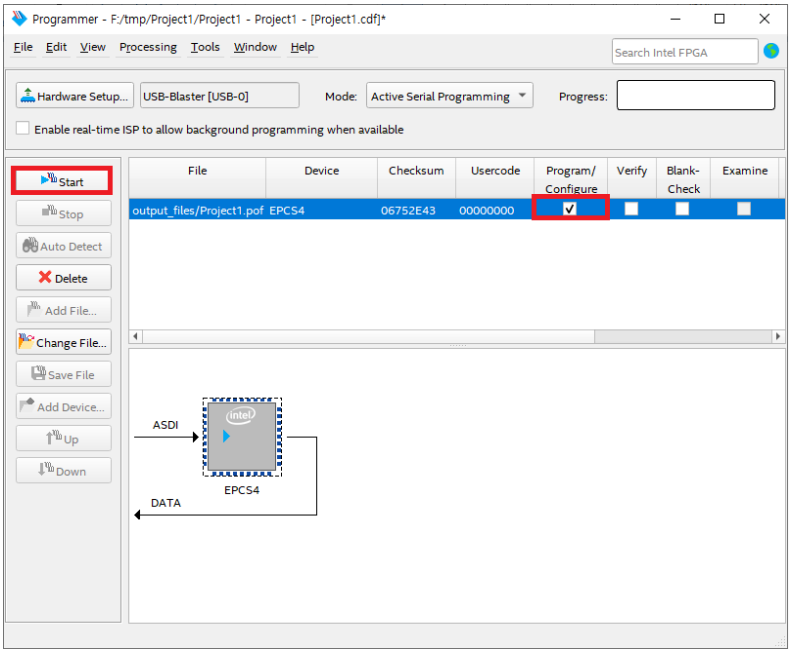
4.4 FPGA에 다운로드

pof FPGA
. pof USB Blaster EPCS4 configuration
, Cyclone IV FPGA . FPGA
USB Blaster USB ,
DIGCOM-A1.2 .

a. Programmer 실행

- [Tools ➔ Programmer] [Programmer]
  Programmer . Programmer Hardware
  Setup ‘USB-Blaster[USB-0]’ , Mode: ‘Active
  Serial Programming’ . [Add
  File...] ‘ \ output_files \ AlteraProject.pof’
  [Open] .
  ‘Program/Configure’ . [Start]
  FPGA .



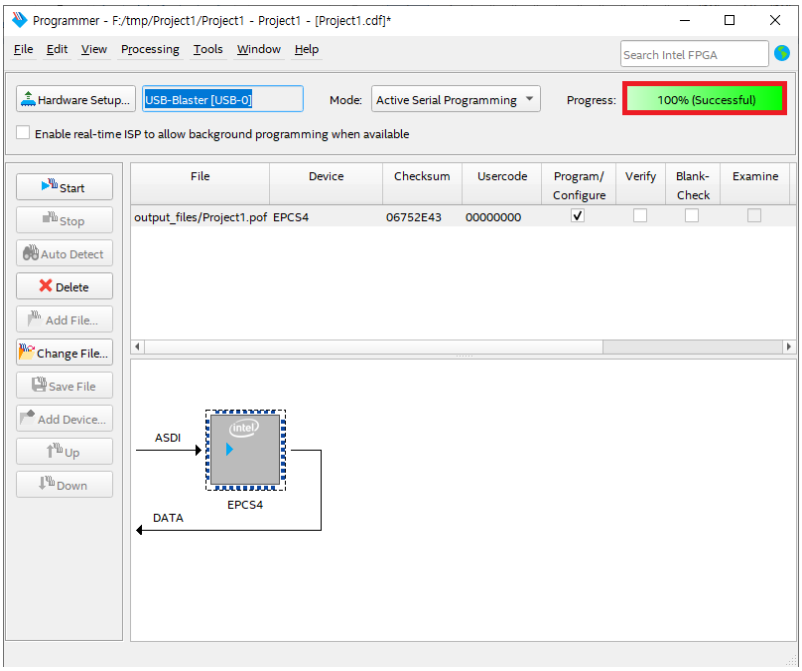


b. **FPGA 다운로드**

- Progress bar ,

DIGCOM-A1.2

.



5. 계층적 프로젝트(Hierarchical Project)

,

.

.

,

Verilog VHDL ,

BSF Block Symbol File .

Block

Diagram/Schematic . schematic ,

BSF

.

4x1 (mux41) VHDL BSF

. VHDL Verilog

Schematic BSF

. Schematic

Verilog VHDL .

4x1 VHDL mux41.BSF ,

mux41 D

. VHDL Verilog 4x1

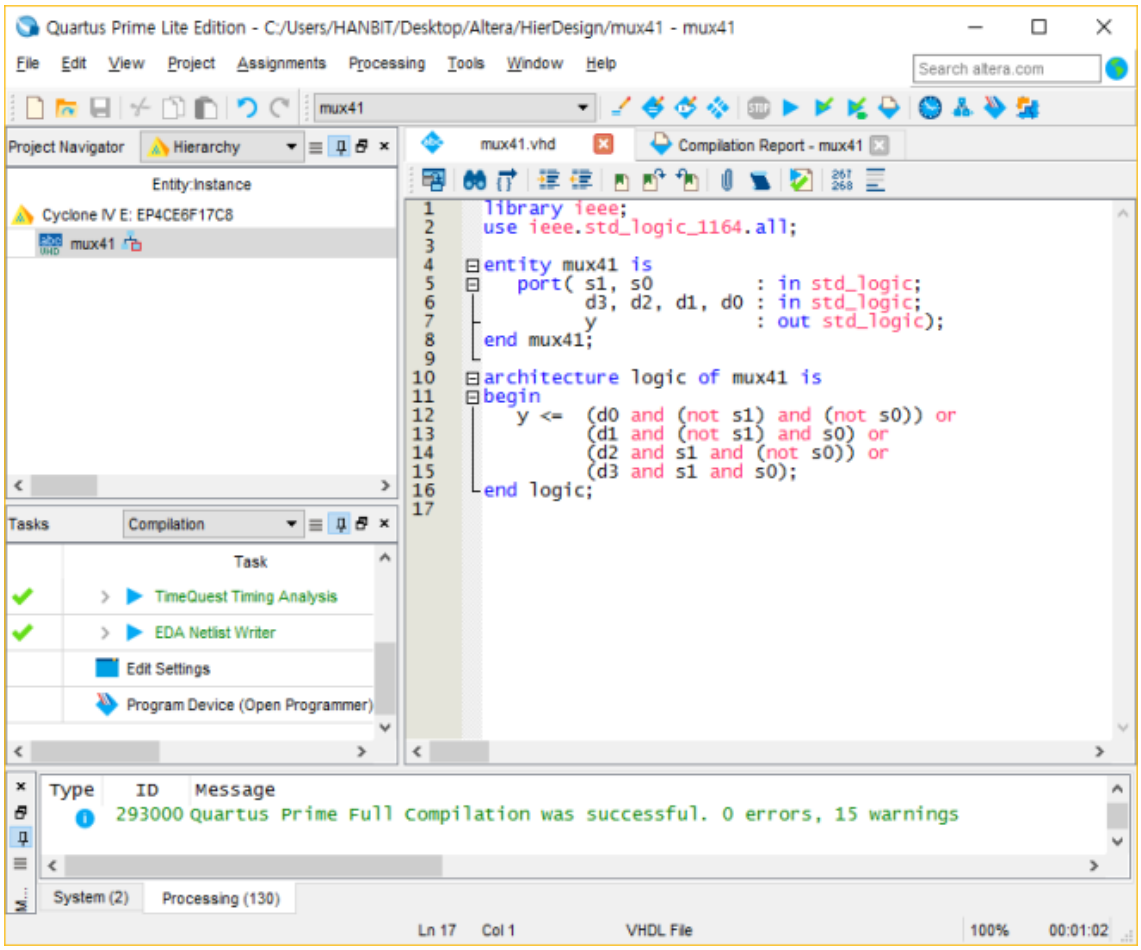
Schematic .

a. **심볼로 생성될 프로젝트 생성**

- HierDesign

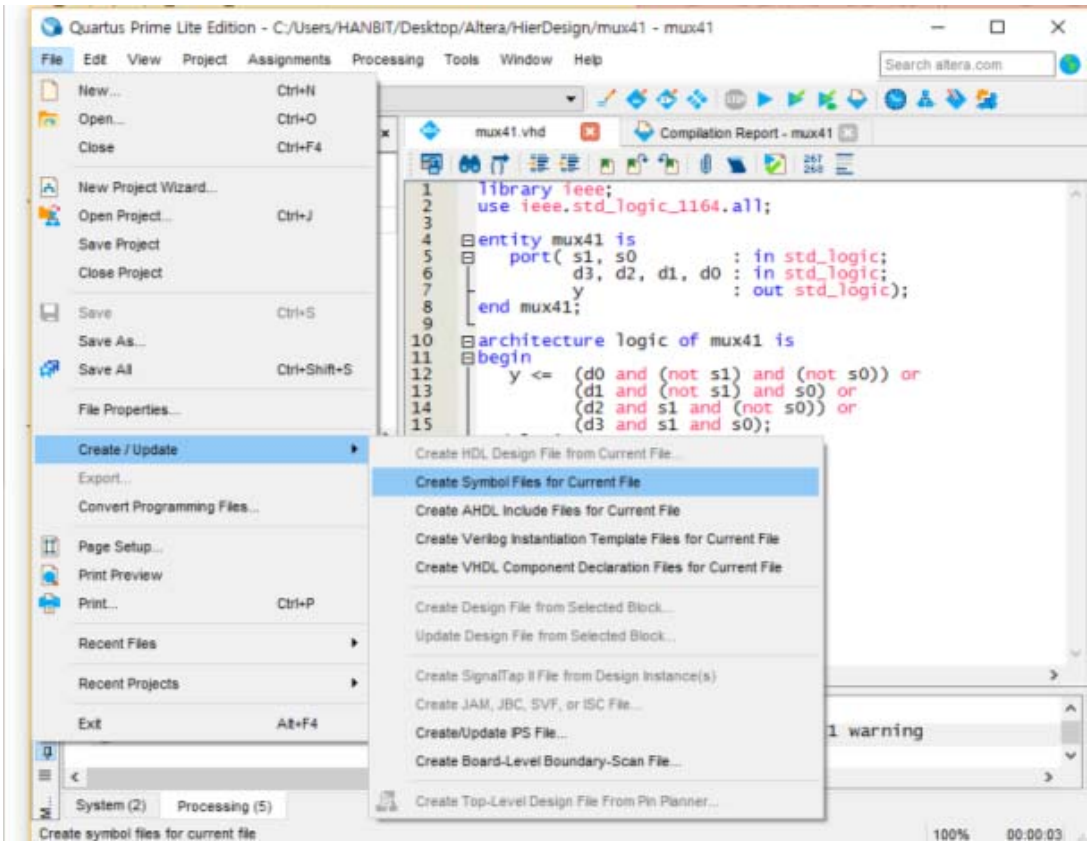
(mux41) . , HierDesign

mux41 mux41. Vhd .



b. **Block Symbol File(BSF) 생성**

- VHDL [File ➔ Create/Update ➔ Create Symbol Files for Current File] Block Symbol File(BSF) .



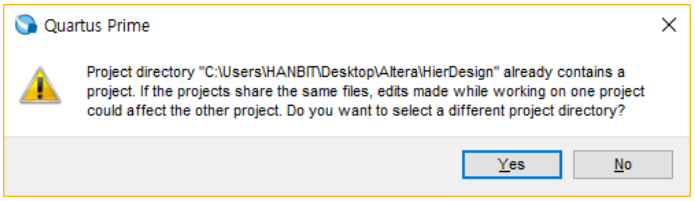
c. **최상위 프로젝트 생성**

- (HierDesign)

.

, [No]

.

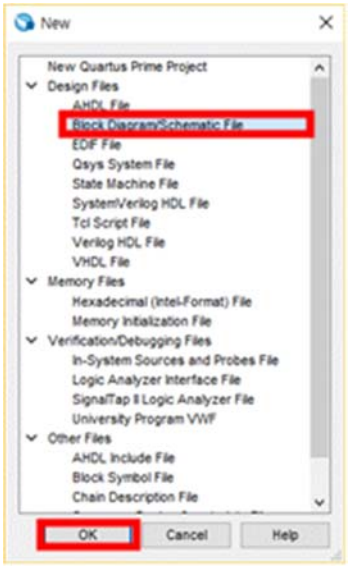


d. **최상위 프로젝트 생성**

- Schematic [File ➔ New ➔ Block Diagram/Schematic File]

. mux41 BSF D

.



e. **mux41 심볼 호출**

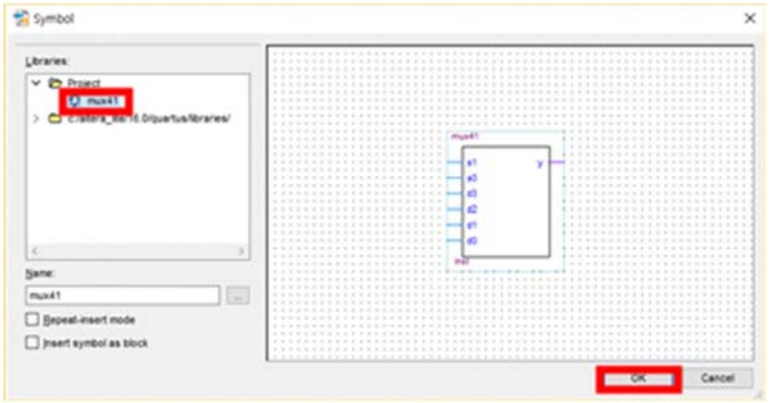
- Schematic Symbol

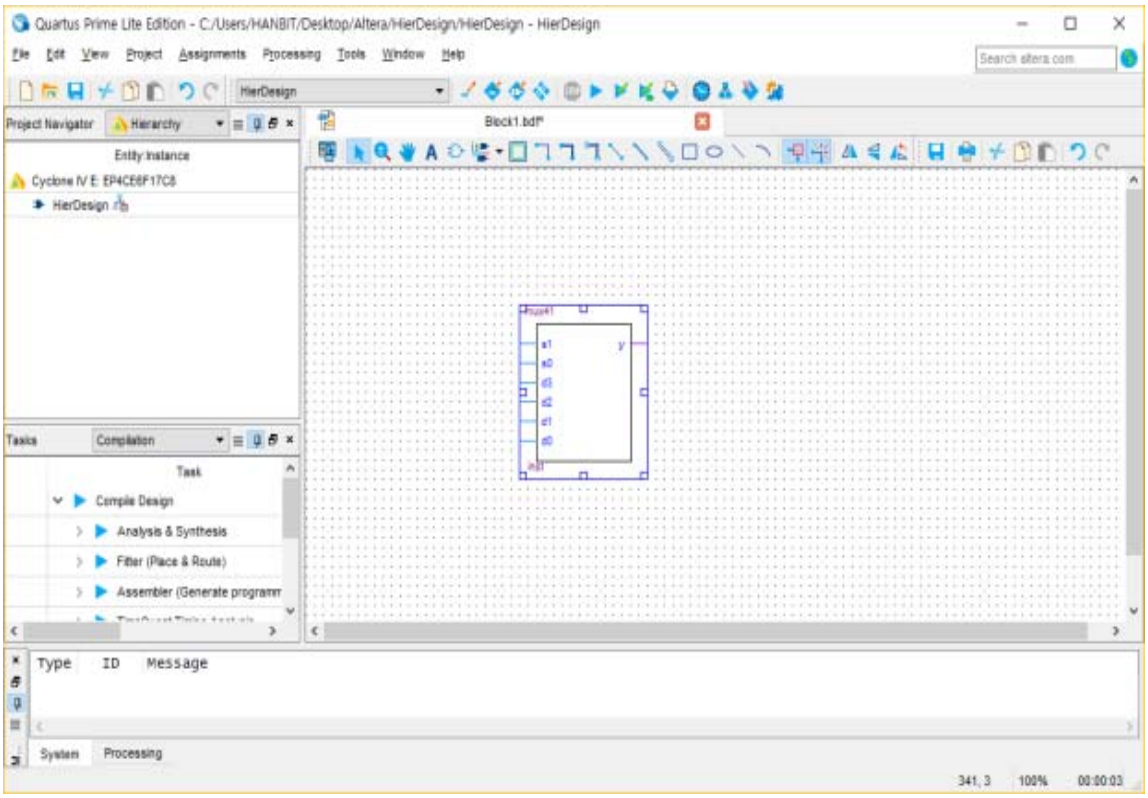
. Libraries: [Project ➔ mux41]

. Project

, . [OK]

.





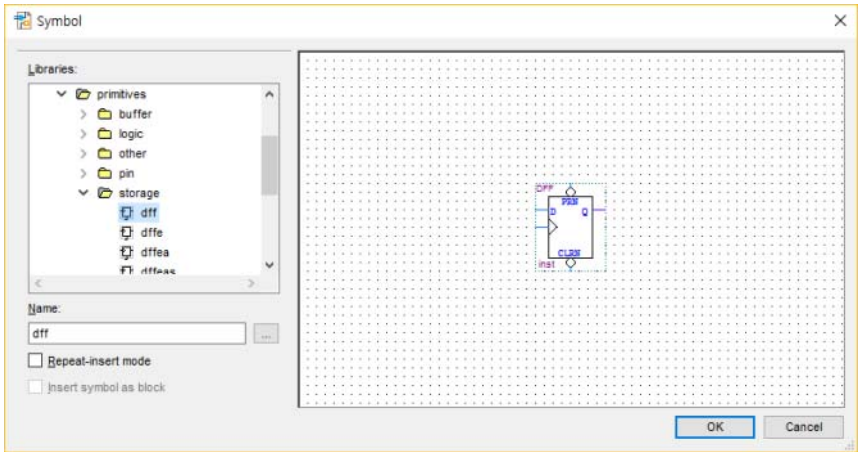
f. **D 플립플롭 호출**

- Schematic

  Symbol . Libraries: [primitives ➔ storage ➔ dff]

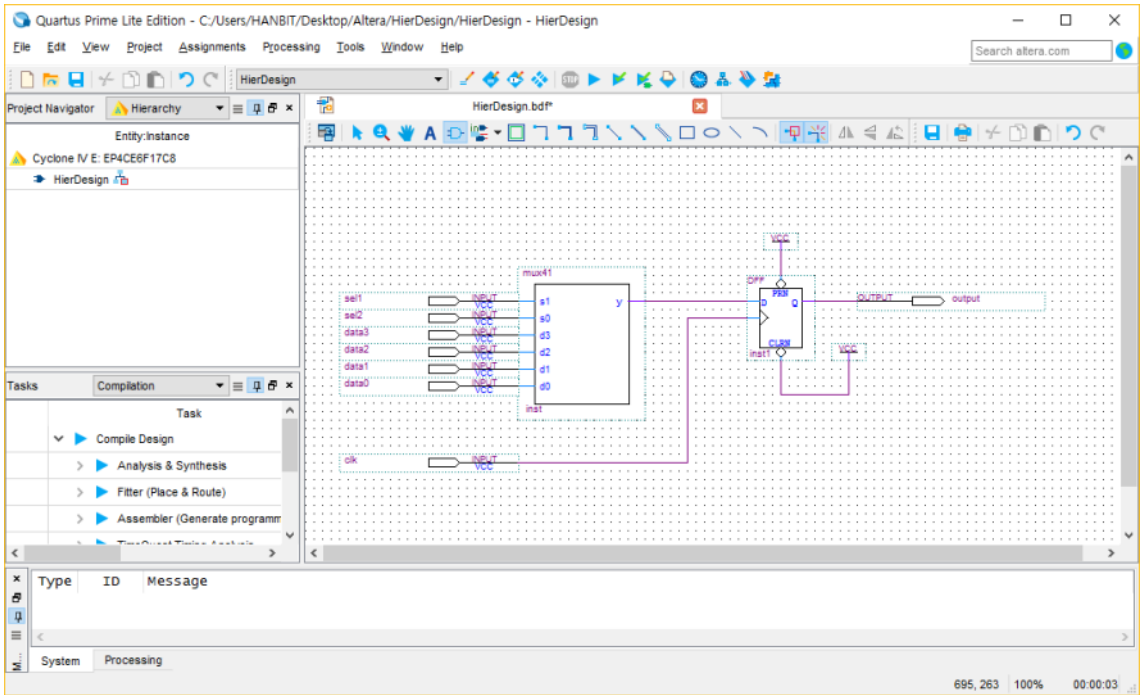
  [OK] . Library

  .



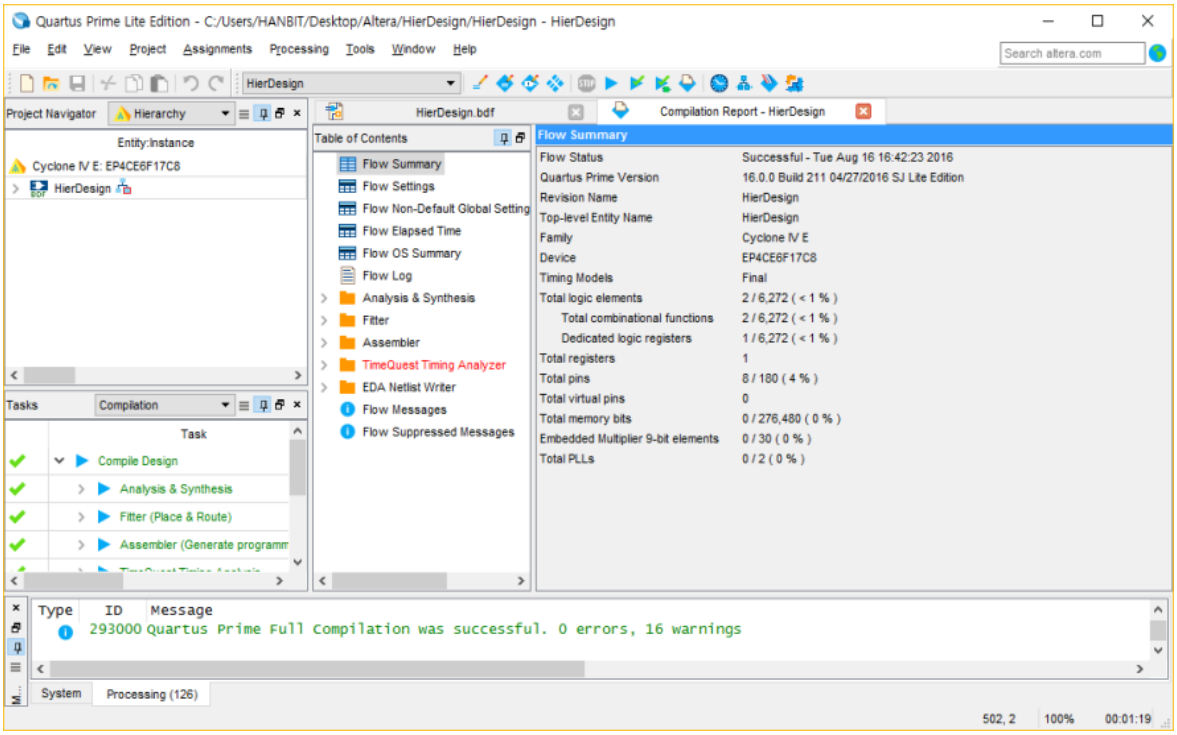
g. D 플립플롭 호출

- ‘HierDesign.bdf’ . input, output , VCC Symbol Symbol .



h. 컴파일 및 FPGA 다운로드

- . FPGA .


Quartus Prime Lite Edition - C:/Users/HANBIT/Desktop/Altera/HierDesign/HierDesign - HierDesign
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
HierDesign
Project Navigator
Hierarchy
Entity:Instance
Cyclone IV E: EP4CE6F17C8
HierDesign
HierDesign.bdf
Compilation Report - HierDesign
Table of Contents
Flow Summary
Flow Settings
Flow Non-Default Global Setting
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Synthesis
Fitter
Assembler
TimeQuest Timing Analyzer
EDA Netlist Writer
Flow Messages
Flow Suppressed Messages
Flow Summary
Flow Status Successful - Tue Aug 16 16:42:23 2016
Quartus Prime Version 16.0.0 Build 211 04/27/2016 SJ Lite Edition
Revision Name HierDesign
Top-level Entity Name HierDesign
Family Cyclone IV E
Device EP4CE6F17C8
Timing Models Final
Total logic elements 2 / 6,272 (< 1 %)
Total combinational functions 2 / 6,272 (< 1 %)
Dedicated logic registers 1 / 6,272 (< 1 %)
Total registers 1
Total pins 8 / 180 (4 %)
Total virtual pins 0
Total memory bits 0 / 276,480 (0 %)
Embedded Multiplier 9-bit elements 0 / 30 (0 %)
Total PLLs 0 / 2 (0 %)
Tasks
Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programm
Type ID Message
293000 Quartus Prime Full Compilation was successful. 0 errors, 16 warnings
System
Processing (126)
502, 2
100%
00:01:19

6. DIGCOM-A1.2 디바이스 핀 할당

a. Device Pin Options 설정

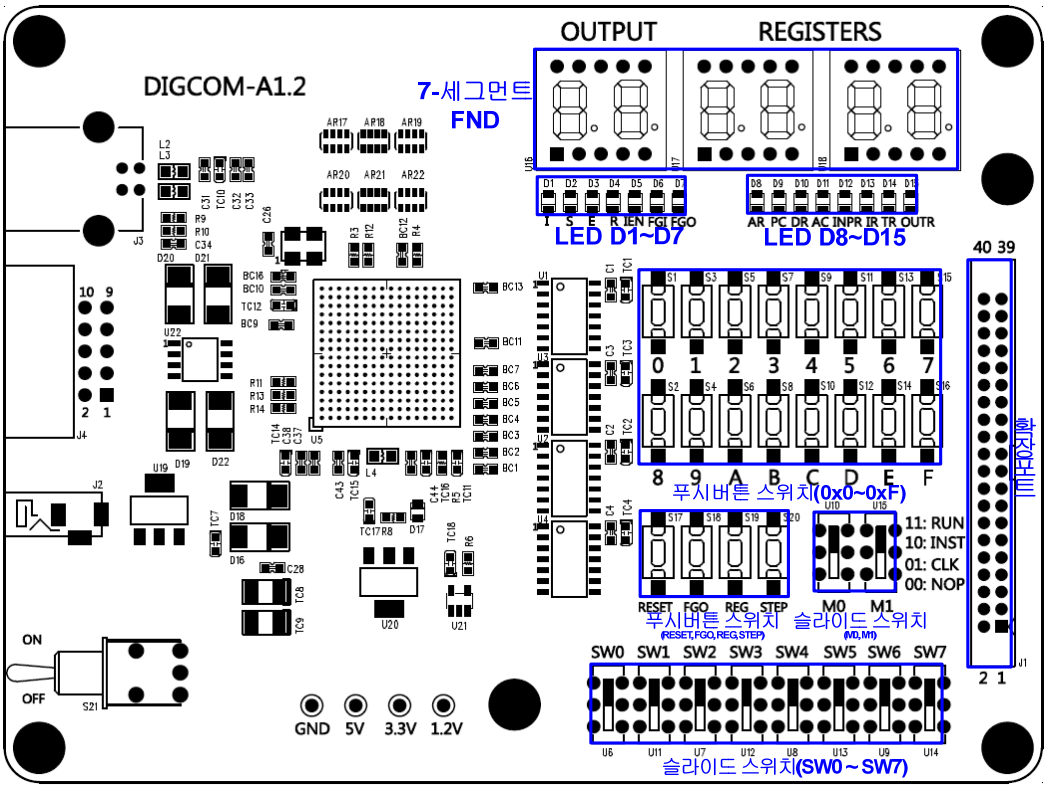
DIGCOM-A1.2 3 2

7- FND, 16 (0x0 ~ 0xF), 4

(RESET, FGO, REG, STEP), 8 (SW0 ~ SW7), 2

(M0, M1) 15 LED(D1 ~ D15) . [3] DIGCOM-A1.2

.



■ (0x0 ~ 0Xf)

0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7
N3	P3	R3	T3	T2	R4	T4	N5
0x8	0x9	0xA	0xB	0xC	0xD	0xE	0xF
N6	M6	P6	M7	K8	R5	T5	R6

■ (RESET, FGO, REG, STEP)

RESET	FGO	REG	STEP
L8	P8	M8	N8

■ (SW0 ~ SW7)

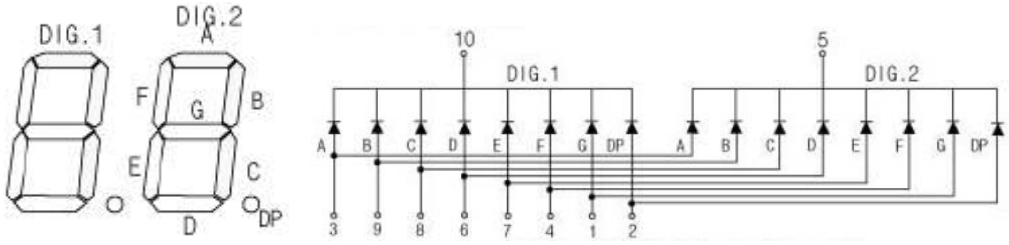
SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
R9	T9	K9	L9	M9	N9	R10	T10

■ (M0, M1)

M0	M1
R12	T12

■ 7- (FND3 ~ FND1)

FND3	FND3A	FND3B	FND3C	FND3D	FND3E	FND3F	FND3G	FND3DP	FND3Sel2	FND3Sel1
	A8	B8	C8	D8	E8	F8	A7	B7	F6	F7
FND2	FND2A	FND2B	FND2C	FND2D	FND2E	FND2F	FND2G	FND2DP	FND2Sel2	FND2Sel1
	C6	A6	B6	E7	E6	A5	A2	B5	A4	B4
FND1	FND1A	FND1B	FND1C	FND1D	FND1E	FND1F	FND1G	FND1DP	FND1Sel2	FND1Sel1
	C14	D14	D11	D12	A13	B13	A14	B14	E11	E10



[그림 4] 2자리 7-세그먼트 FND 핀 배열

■ LED(D1 ~ D7)

D1	D2	D3	D4	D5	D6	D7
A12	B12	A11	B11	C11	F10	F9

■ LED(D8 ~ D15)

D8	D9	D10	D11	D12	D13	D14	D15
F11	A15	A10	B10	C9	D9	E9	A9

■ (IO0 ~IO31)

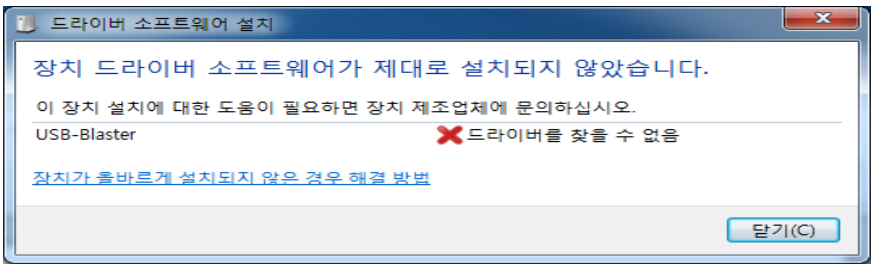
IO0	IO1	IO2	IO3	IO4	IO5	IO6	IO7
N13	M12	L12	K12	N14	P15	P16	R16
IO8	IO9	IO10	IO11	IO12	IO13	IO14	IO15
K11	N16	N15	L14	L13	L16	L15	J11
IO16	IO17	IO18	IO19	IO20	IO21	IO22	IO23
K16	K15	J16	J15	J14	J12	J13	G16
IO24	IO25	IO26	IO27	IO28	IO29	IO30	IO31
G15	F13	G11	F15	B16	F14	D16	D15

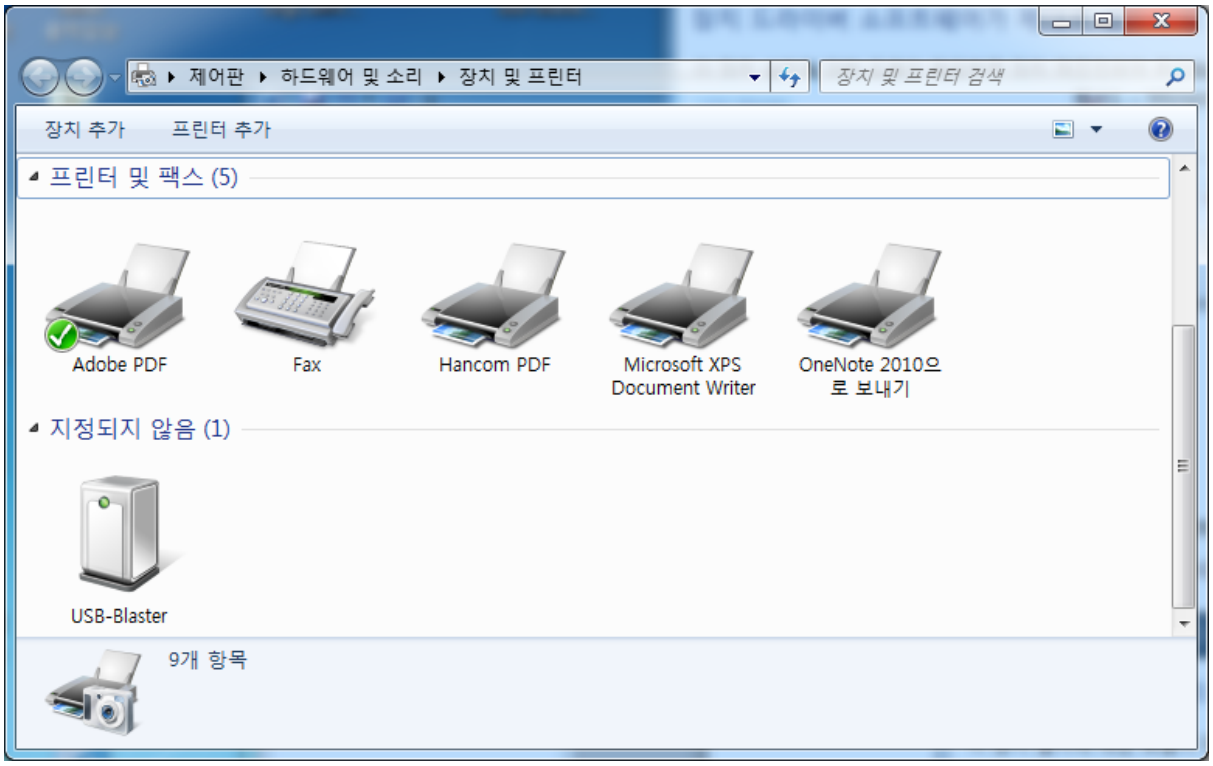
■ Oscillator : E16, E15

7. USB-Blaster 드라이버 설치(64비트 윈도우10 기준)

Usb blaster ,

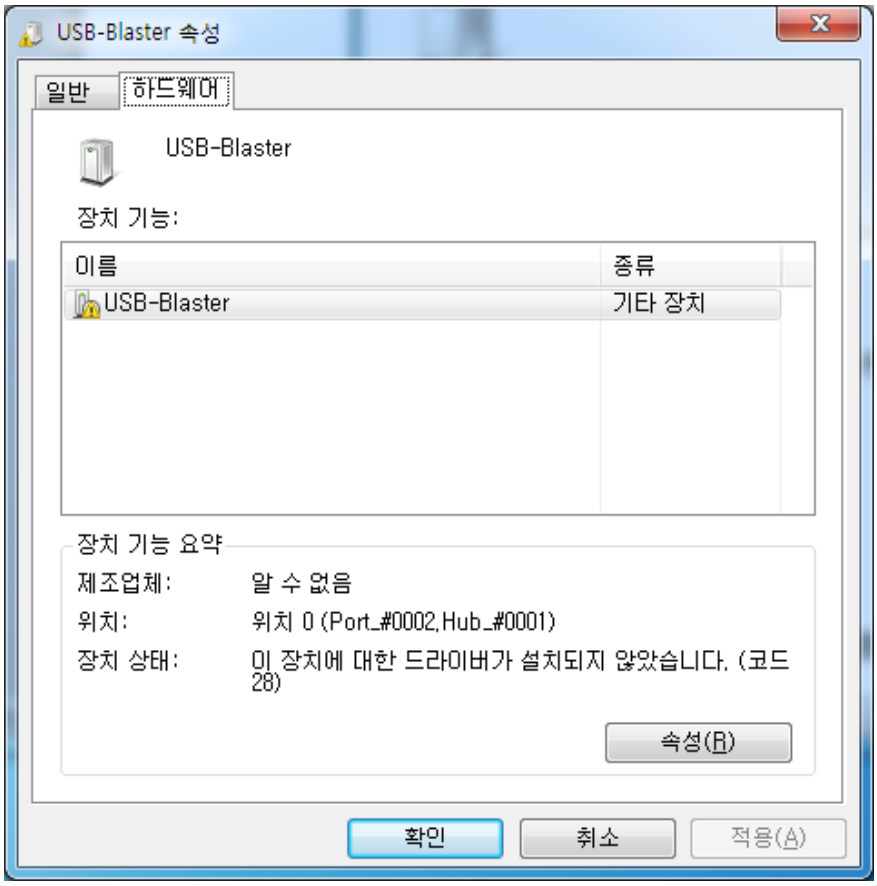
USB-BLASTER “ ” .



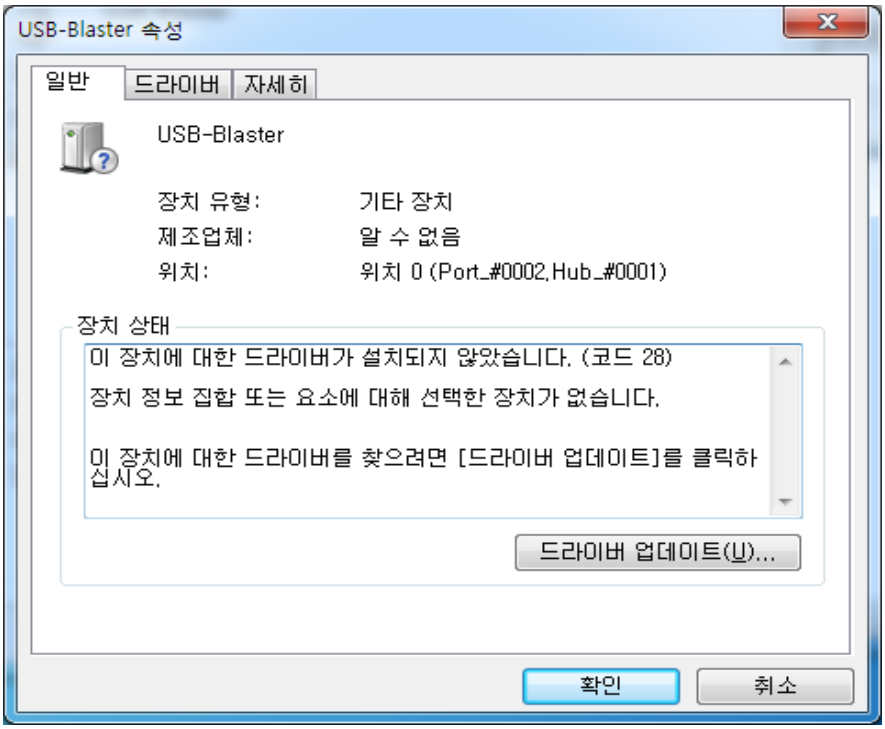


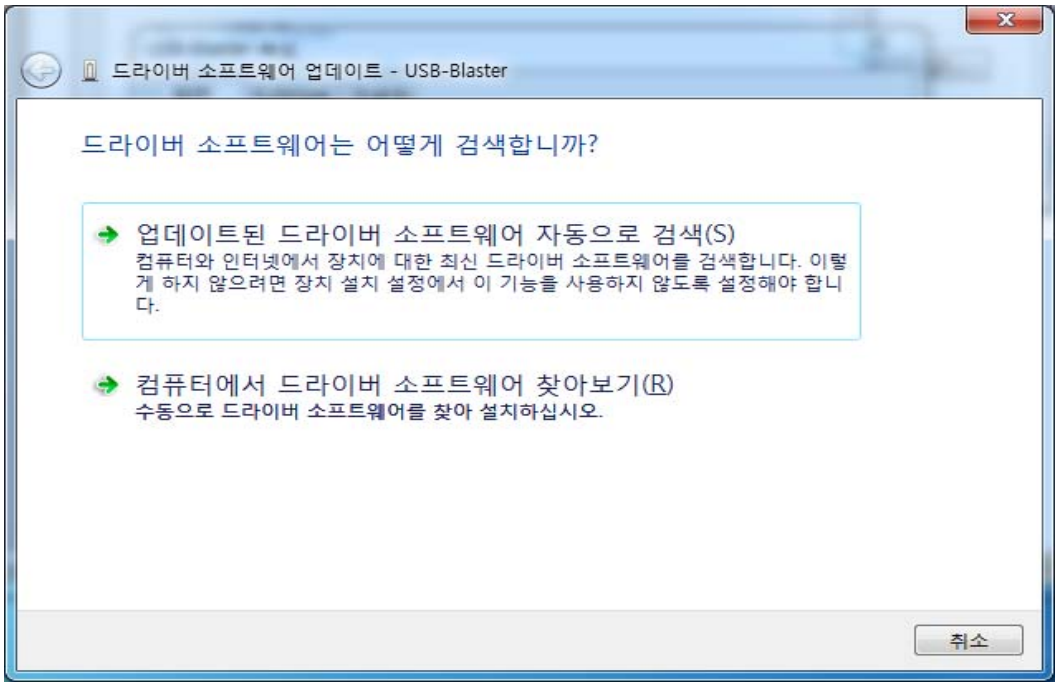
Usb blaster

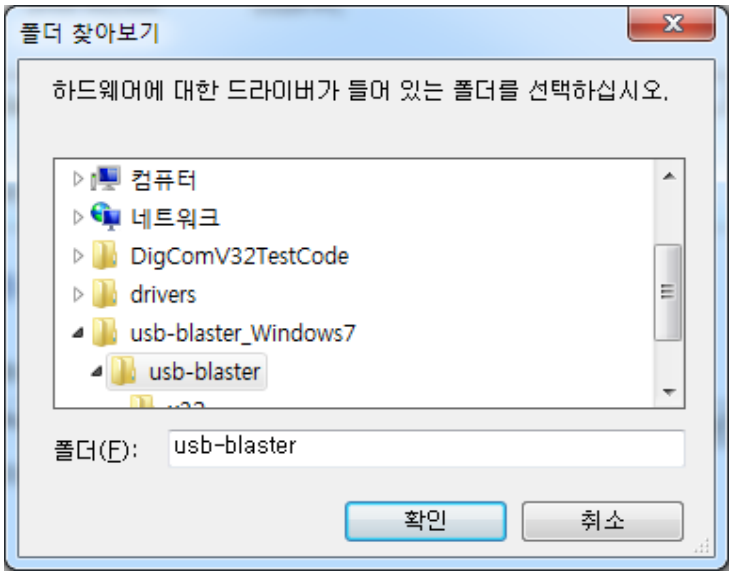
Usb-blaster , .


USB-Blaster 속성
일반
하드웨어
USB-Blaster
장치 기능:
이름
종류
USB-Blaster
기타 장치
장치 기능 요약
제조업체:
알 수 없음
위치:
위치 0 (Port_#0002,Hub_#0001)
장치 상태:
이 장치에 대한 드라이버가 설치되지 않았습니다. (코드 28)
속성(R)
확인
취소
적용(A)

.

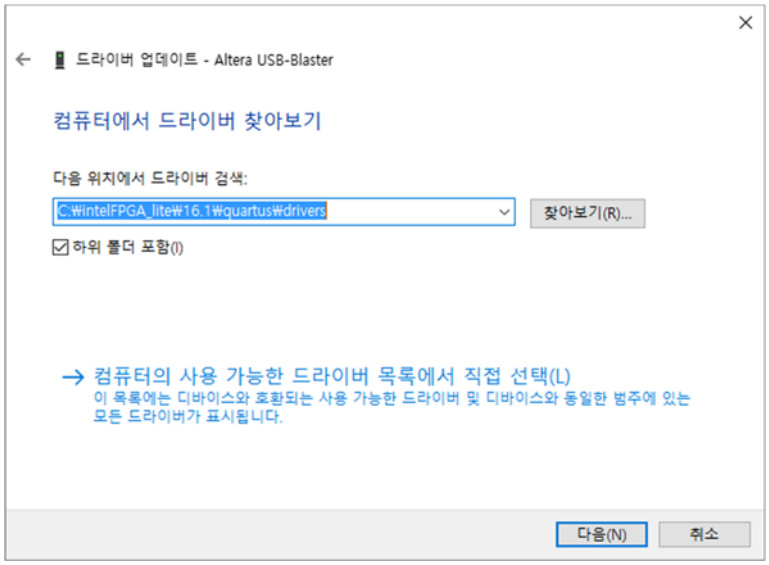

USB-Blaster 속성
일반
드라이버
자세히
USB-Blaster
장치 유형:
기타 장치
제조업체:
알 수 없음
위치:
위치 0 (Port_#0002,Hub_#0001)
장치 상태
이 장치에 대한 드라이버가 설치되지 않았습니다. (코드 28)
장치 정보 집합 또는 요소에 대해 선택한 장치가 없습니다.
이 장치에 대한 드라이버를 찾으려면 [드라이버 업데이트]를 클릭하십시오.
드라이버 업데이트(U)...
확인
취소


드라이버 소프트웨어 업데이트 - USB-Blaster
드라이버 소프트웨어는 어떻게 검색합니까?
업데이트된 드라이버 소프트웨어 자동으로 검색(S)
컴퓨터와 인터넷에서 장치에 대한 최신 드라이버 소프트웨어를 검색합니다. 이렇게 하지 않으려면 장치 설치 설정에서 이 기능을 사용하지 않도록 설정해야 합니다.
컴퓨터에서 드라이버 소프트웨어 찾아보기(R)
수동으로 드라이버 소프트웨어를 찾아 설치하십시오.
취소

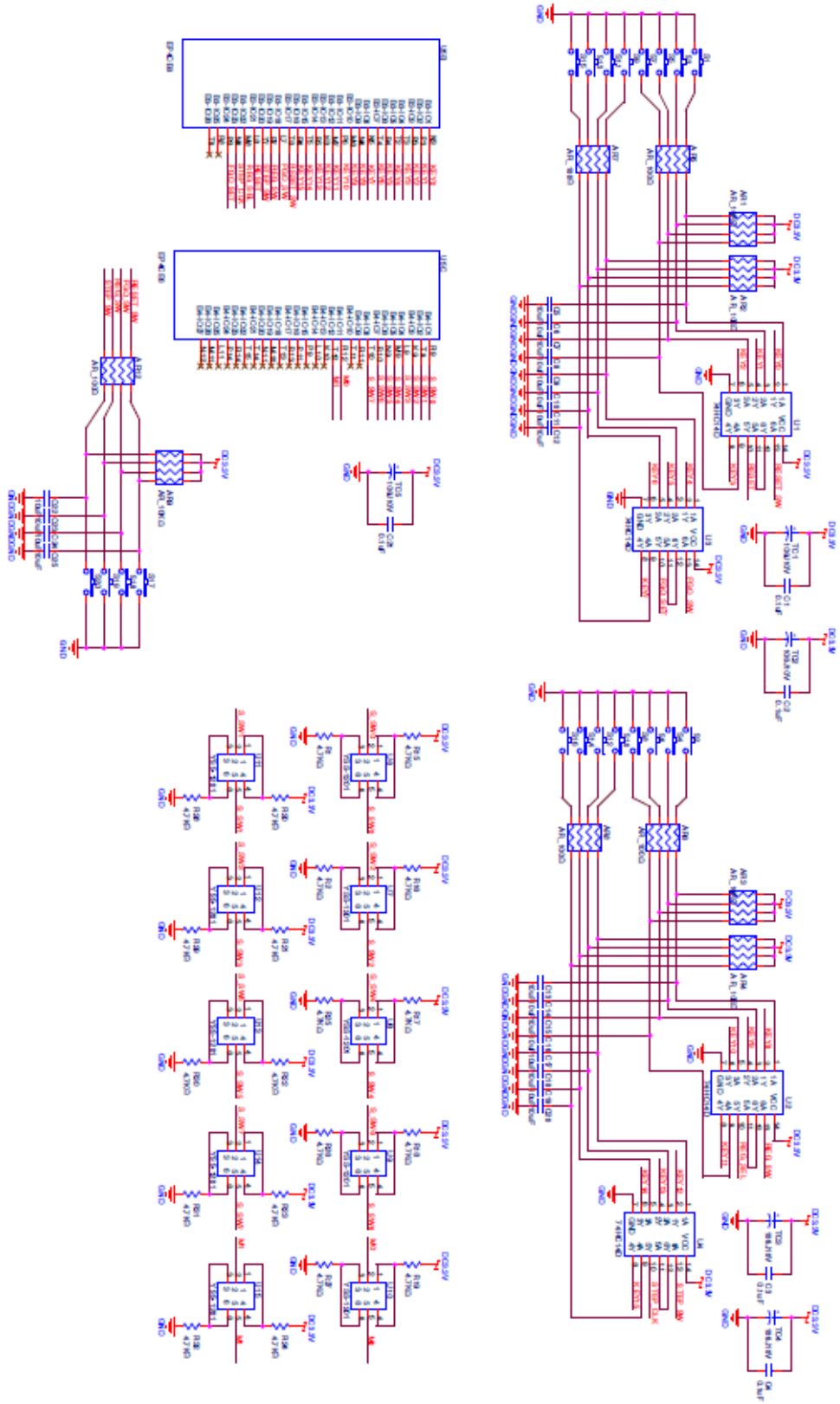

폴더 찾아보기
하드웨어에 대한 드라이버가 들어 있는 폴더를 선택하십시오.
컴퓨터
네트워크
DigComV32TestCode
drivers
usb-blaster_Windows7
usb-blaster
폴더(F):
usb-blaster
확인
취소

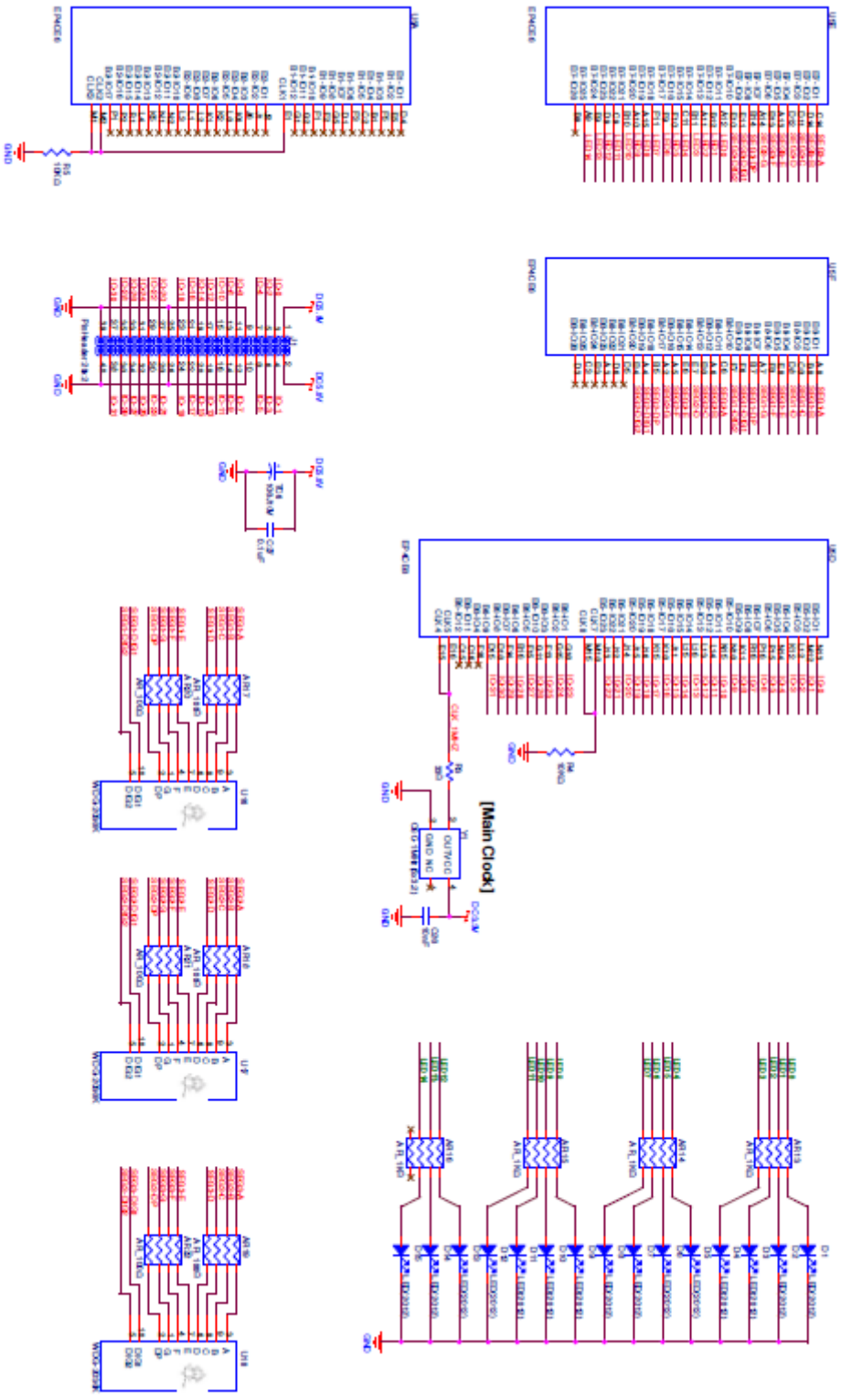
C: \ intelFPGA_lite \ 16.1 \ quartus \ drivers

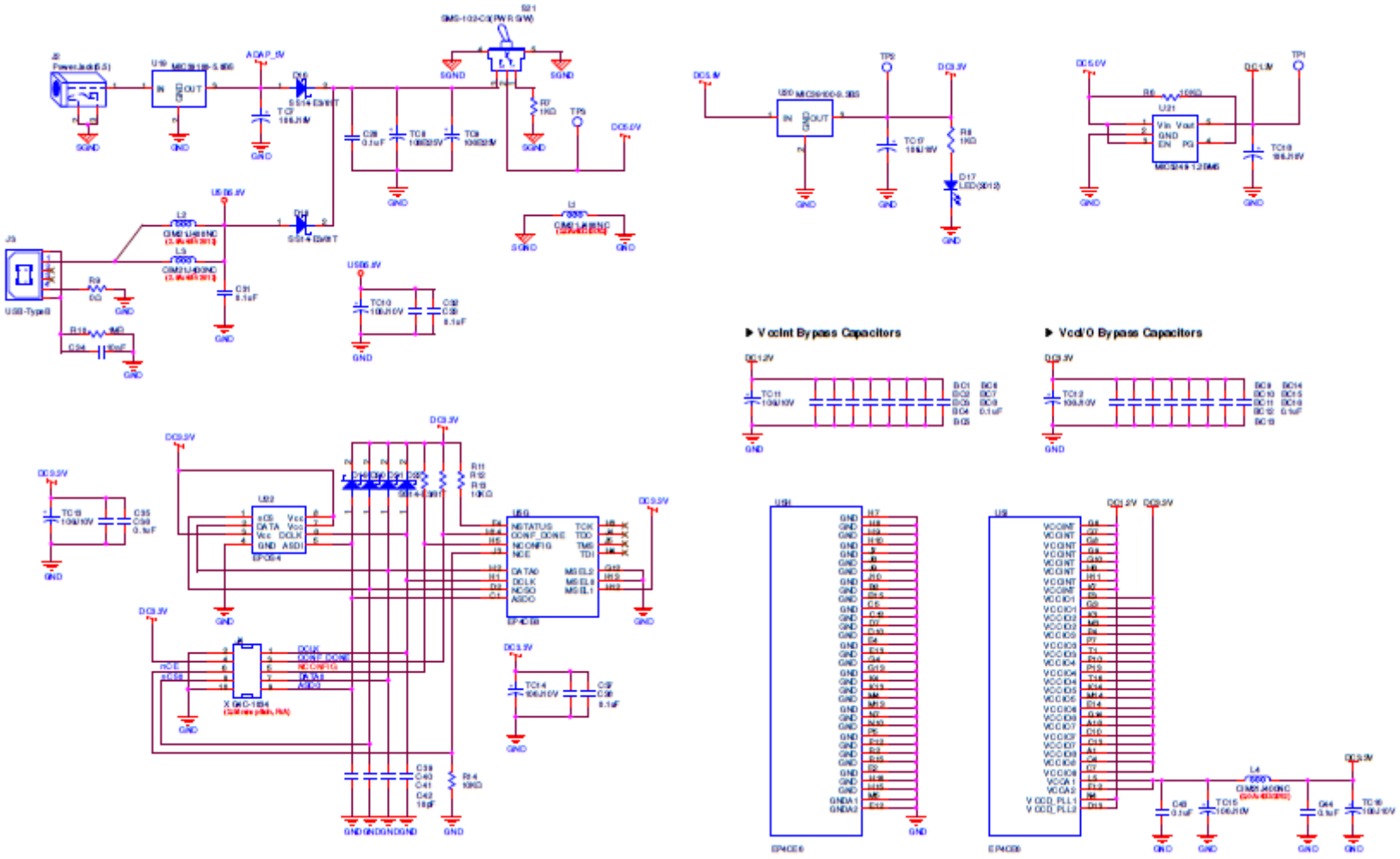
.



8. DIGCOM-A1.2 회로도




[Main Clock]


▶ Vccint Bypass Capacitors
▶ Vccl/O Bypass Capacitors