

▷ DIGCOM XA(Xilinx-Artix) Board V1.1

※ 수정사항

- Ver1.0 [2017.03.16]

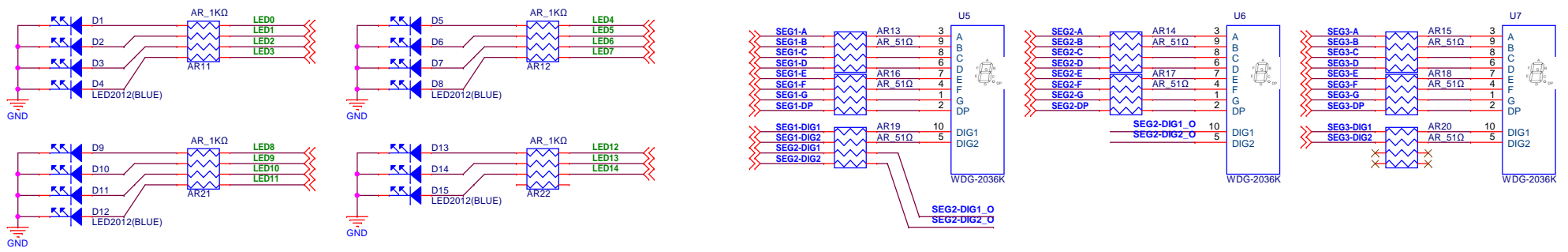
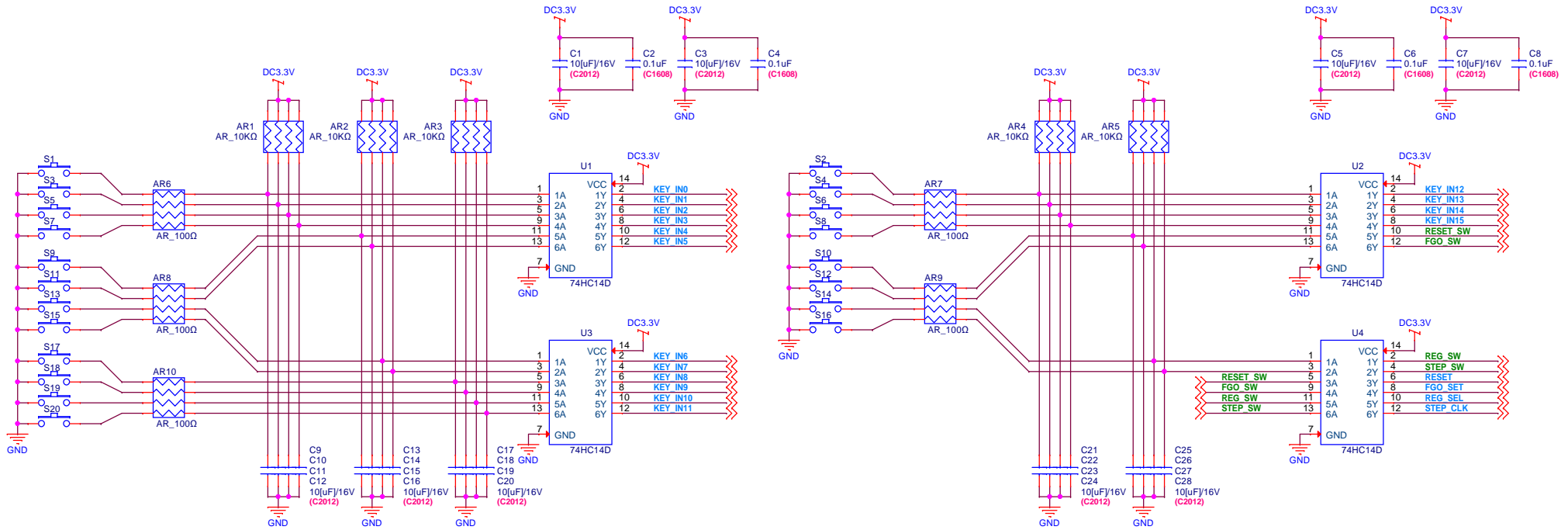
1. 보판 수정 : DIGCOM- X2. 0 -> DIGCOM-XA 0
2. J2 커넥터의 Pin 이동 배치 지참
3. LED Silk 콘테로 정렬 배치 지참
4. U21,U22 부품 Thermal P 어부분에 Variat메스 고려)
5. 4page GNDADC 분배 추가
6. "USB+5V" Silk 분열에 F 어크지수정
7. C46과 R35 실드면 경

- Ver1.1 [2022.11.30]

1. 00page, History 쿼 및 01pag 수정 사항에 이 지로 이동
2. 03page, F3, F4변 RS232_RXD , RS232_TX 라인 제거
3. 04page, J2 socket 게, TMS , TCK , TDI , TDO Off-page e connect
4. 05page, USB Type-B 원부제거 , USB Ty e C입력 외 수정
5. 05page, PowerJack 원부제거 캐피터 추가
6. 05page, 전 LE D배상 RDI 변경 , regulator BU1 D로 변경
7. 05page, USB to UART Bridge 제
8. 06page, Platform Cable 카

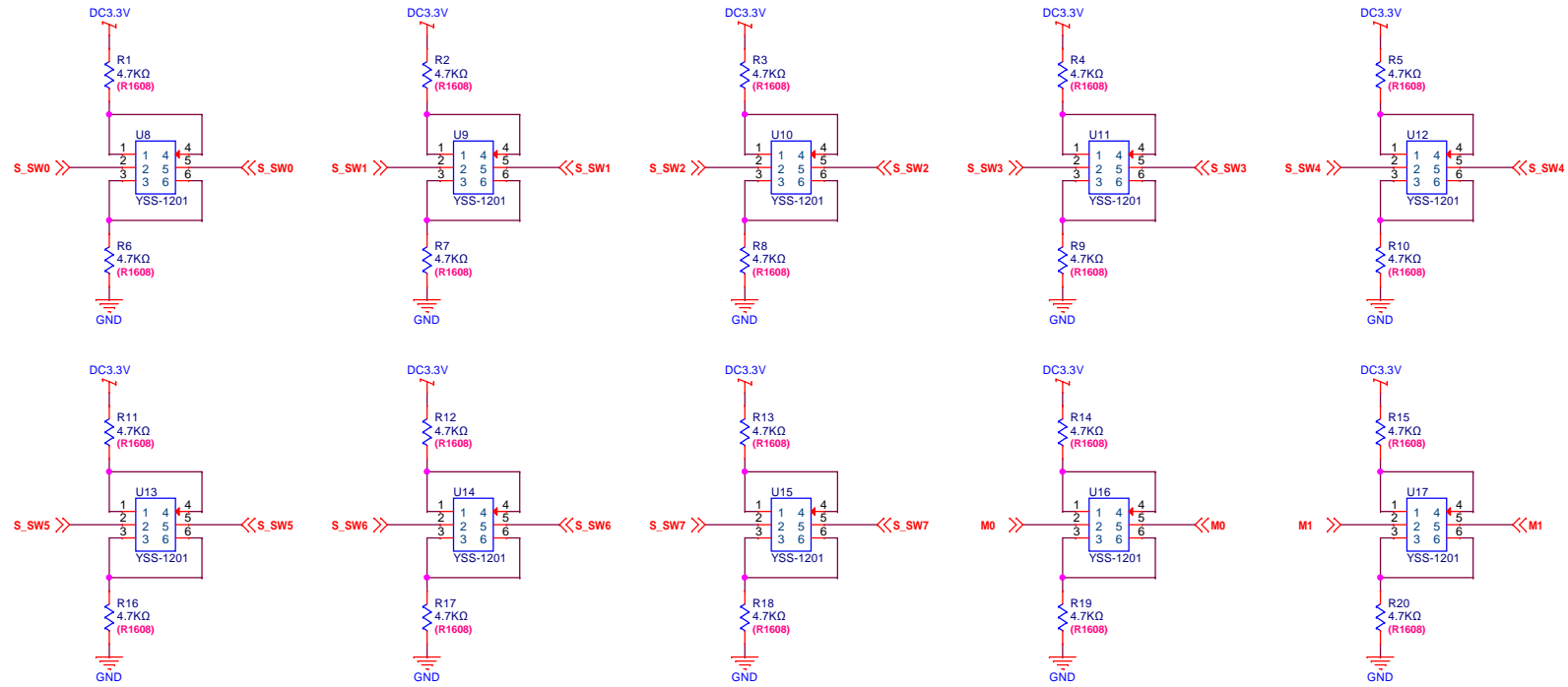
Title		
▷ DIGCOM XA(Xilinx-Artix) Board V1.1		
Size	Document Number	Rev
A3	History	1.1
Date:	Wednesday, August 23, 2023	Sheet 1 of 7

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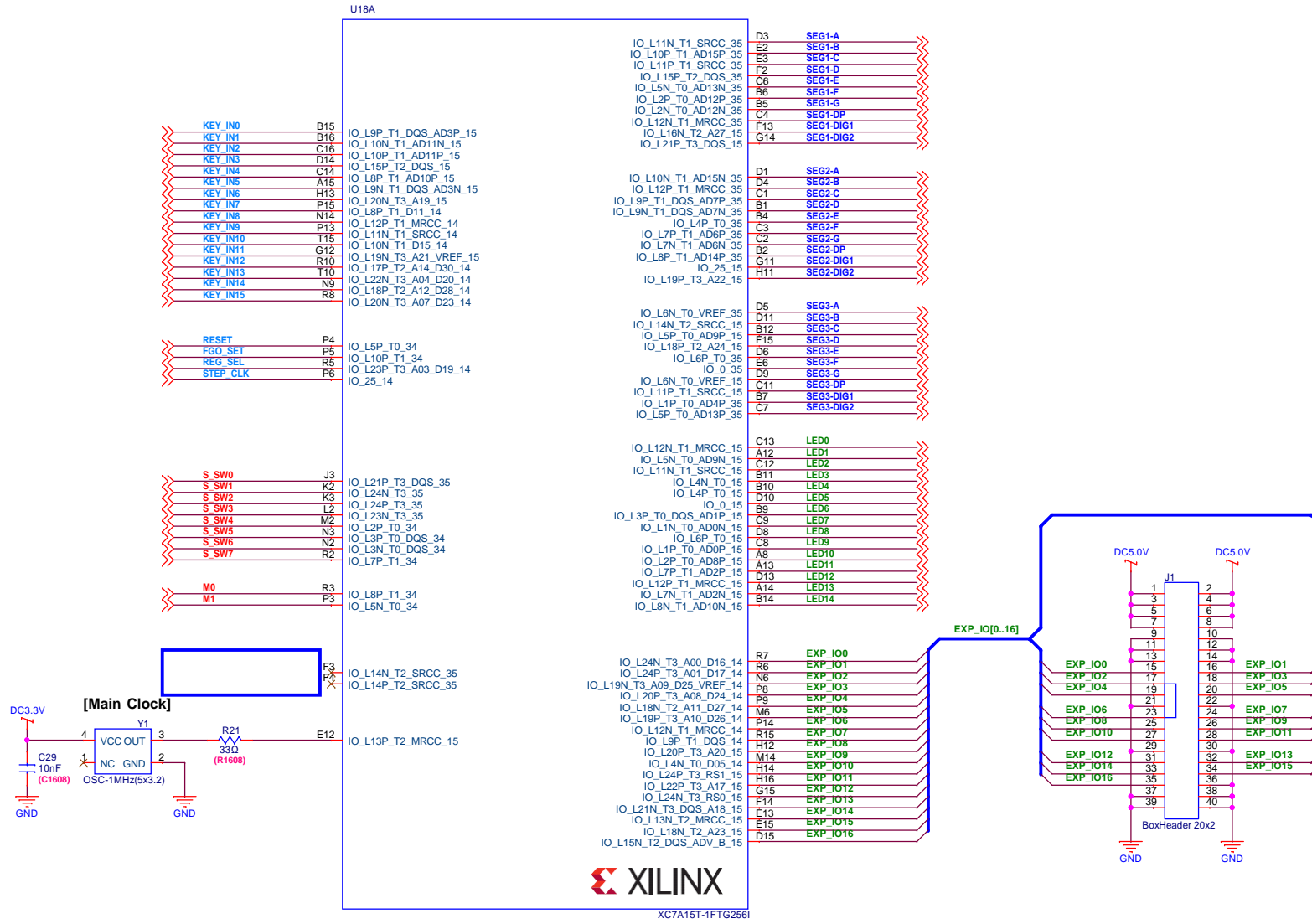
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▷ DIGCOM XA(Xilinx-Artix) Board V1.1		
Size	Document Number	Rev
A3	Push Key and LED, 7-Segment Interface	1.1
Date:	Wednesday, August 23, 2023	Sheet 2 of 7

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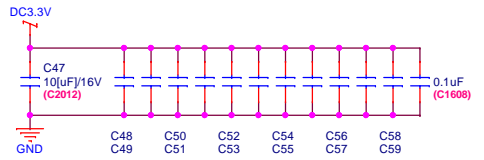
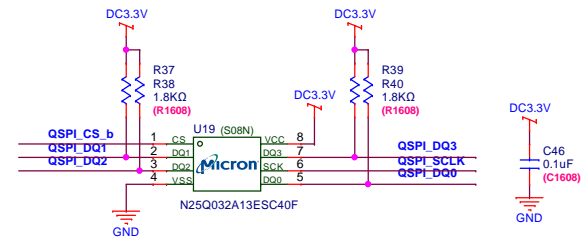
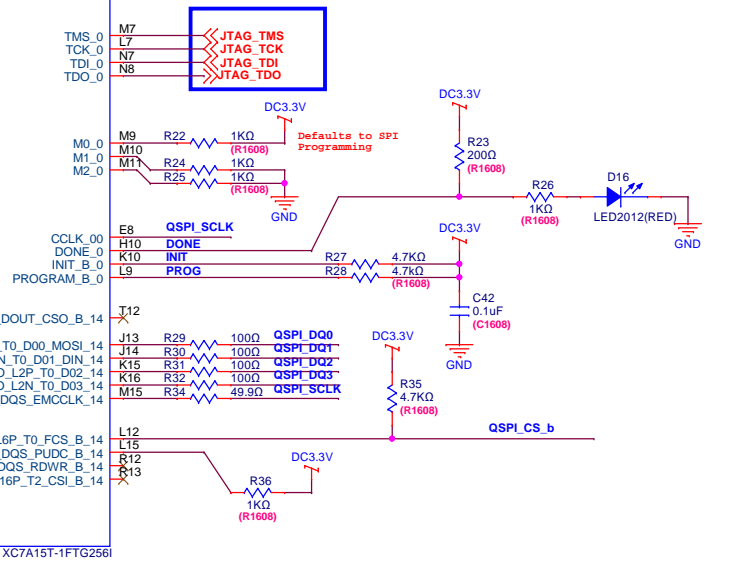
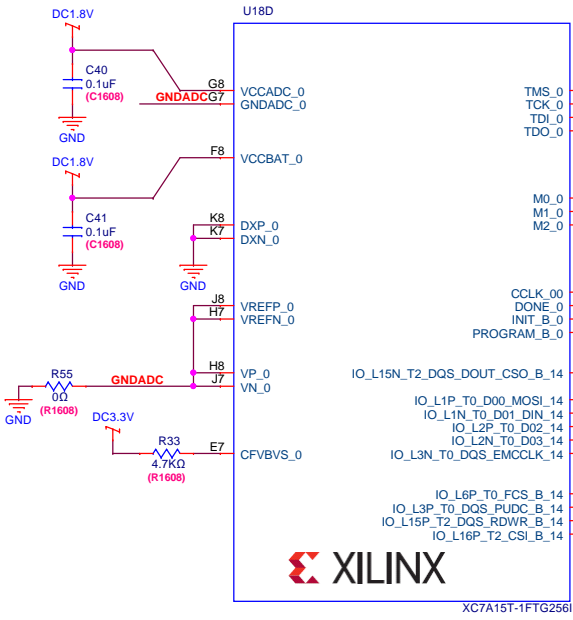
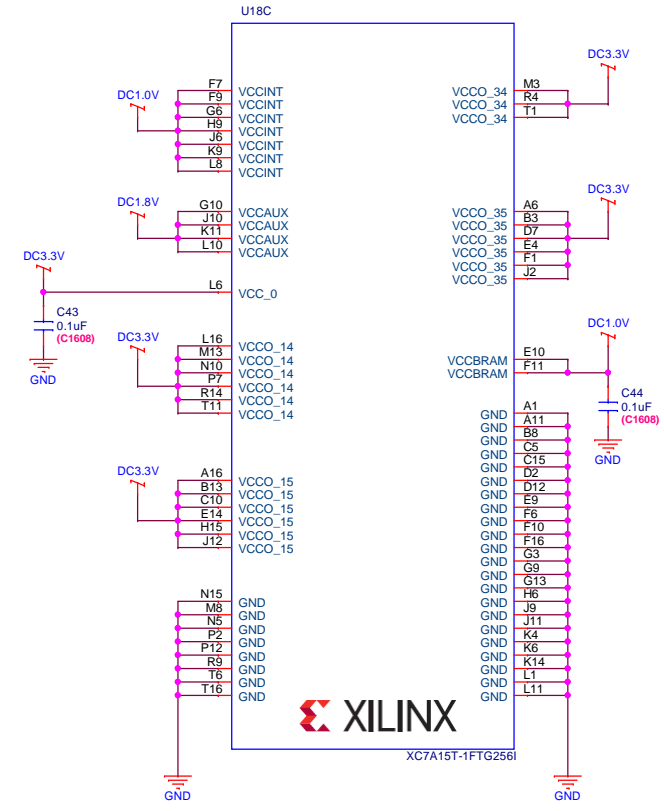
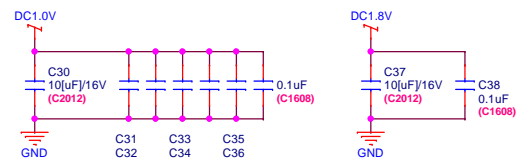


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▷ DIGCOM XA(Xilinx-Artix) Board V1.1		
Size	Document Number	Rev
A3	Slide Switch Interface	1.1
Date:	Wednesday, August 23, 2023	Sheet 3 of 7

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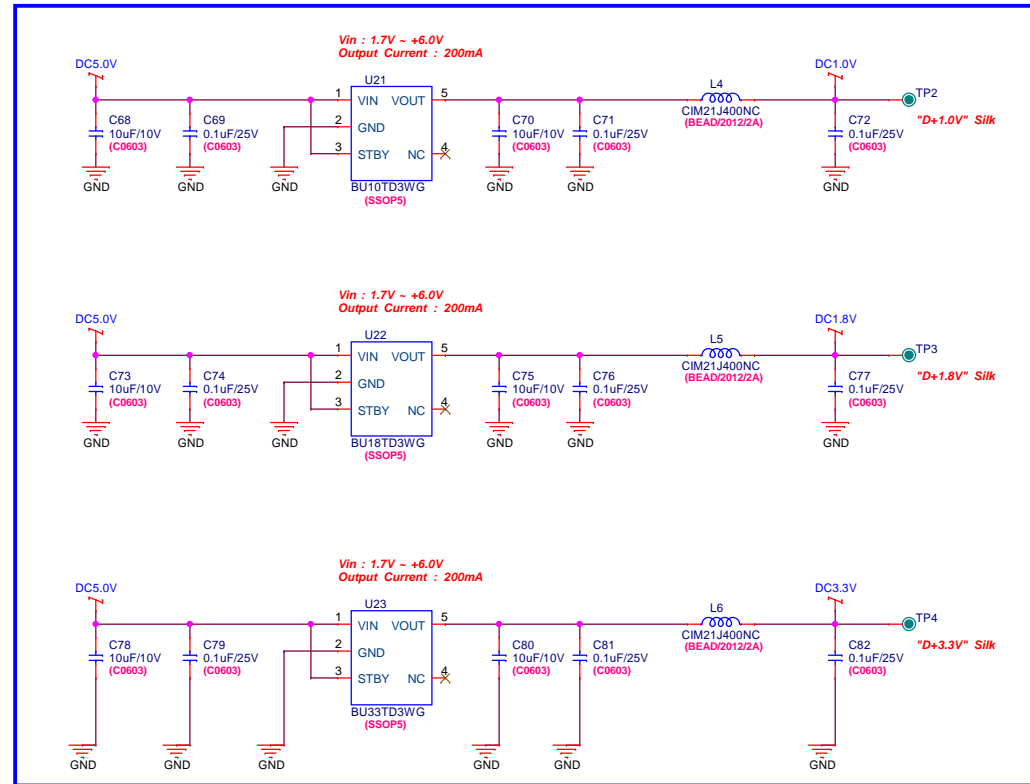
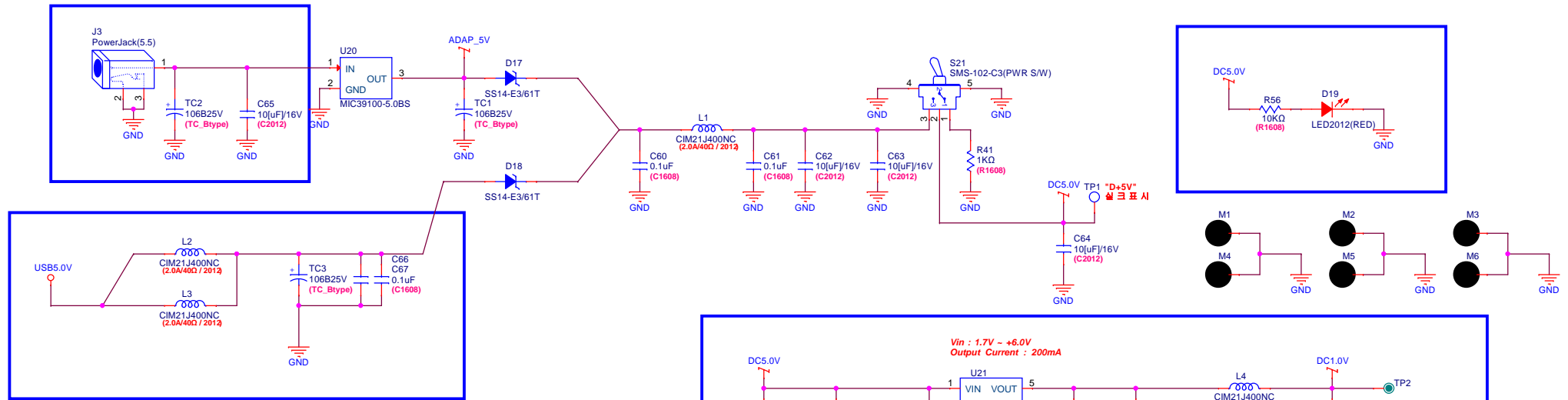


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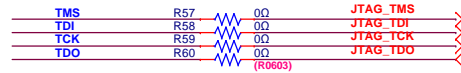
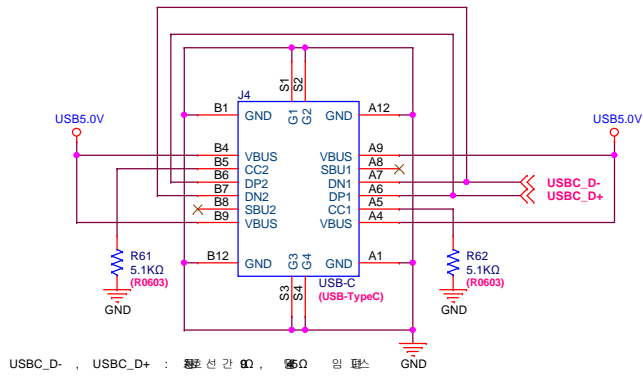
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▷ DIGCOM XA(Xilinx-Artix) Board V1.1		
Size	Document Number	Rev
A3	FPGA JTAG and Core Interface	1.1
Date:	Wednesday, August 23, 2023	Sheet 5 of 7

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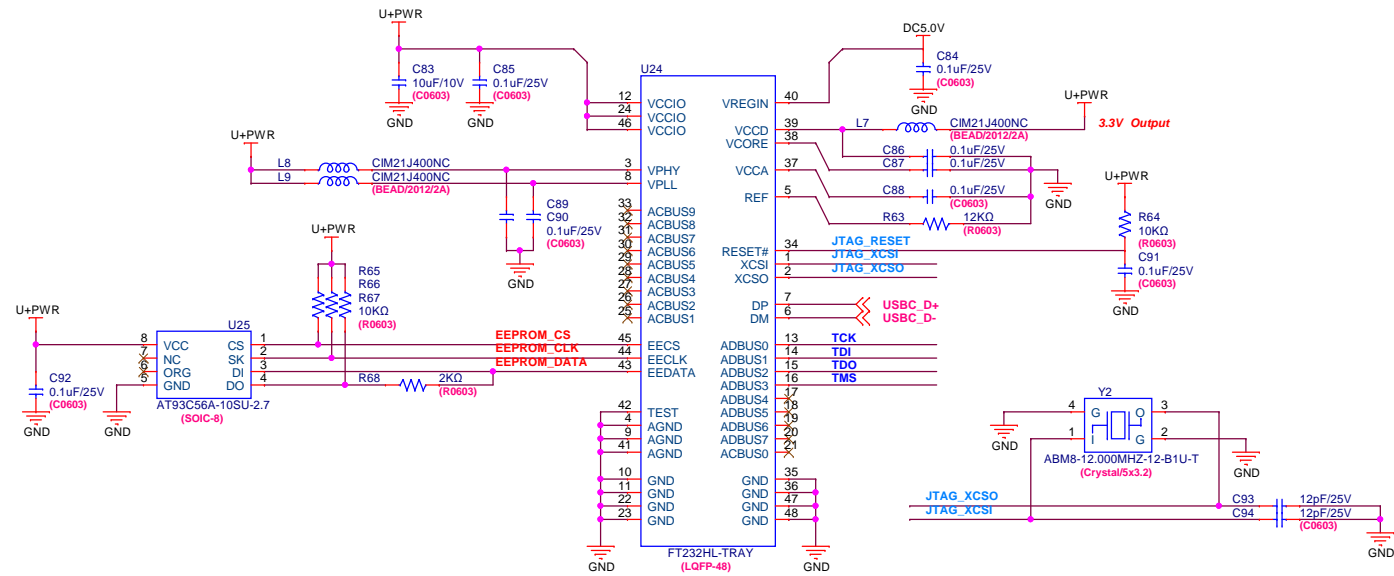


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▷ DIGCOM XA(Xilinx-Artix) Board V1.1		
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A3	Power Interface	1.1
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USBC_D-, USBC_D+ : 5.1kΩ, 5.1kΩ 임피던스



Title		
▷ DIGCOM XA(Xilinx-Artix) Board V1.1		
Size	Document Number	Rev
A3	Platform Cable Interface	1.1
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