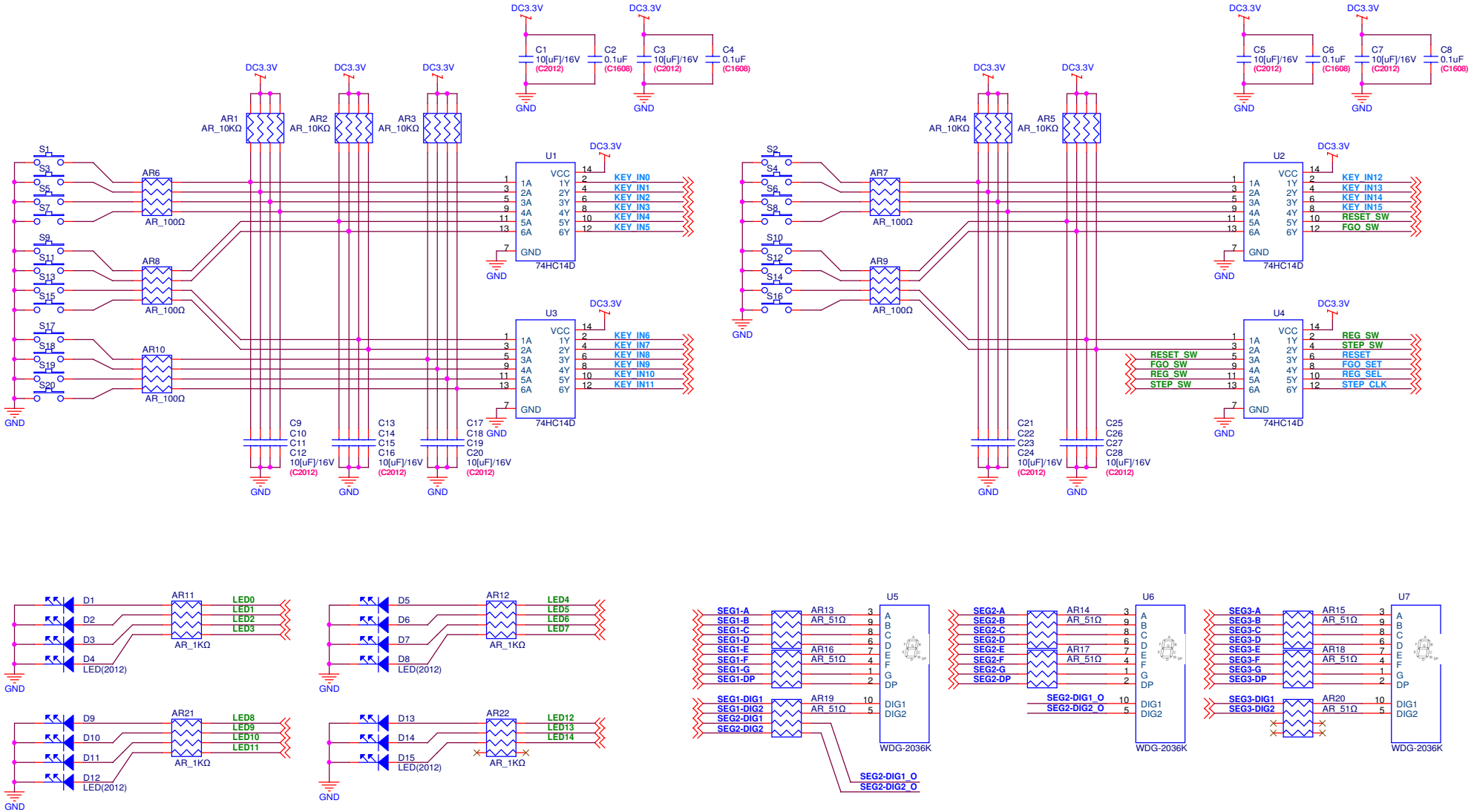
※ 수정사항

- Ver1.0 [2017.03.16]

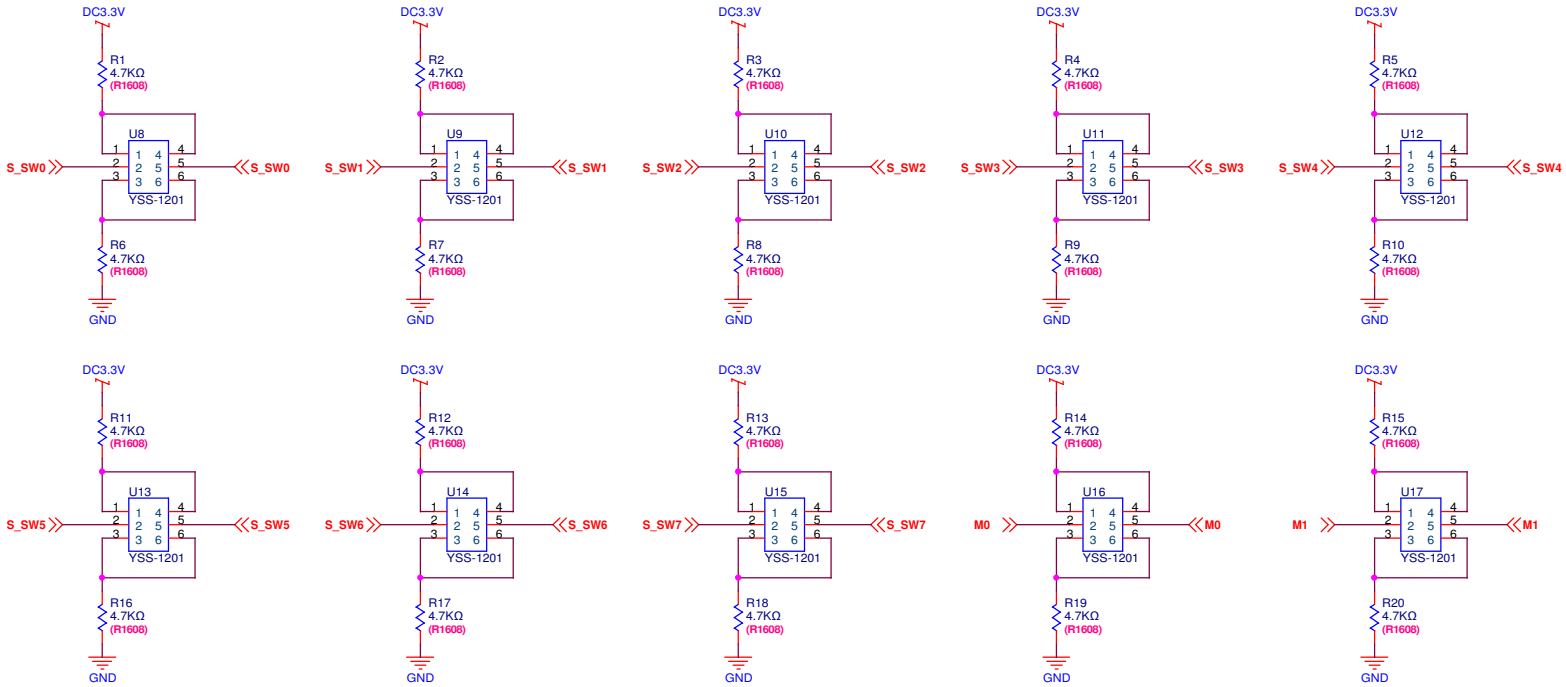
1. 보드명 수정 : DIGCOM-X2.0 -> DIGCOM-XA1.0
2. J2커넥터 외곽으로 1mm 이동배치
3. LED Silk 순서대로 정렬(1페이지 참조)
4. U21,U22번 부품 Thermal Pad 부분에 Via 추가(열패스 고려)
5. 4page GNDADC 부분 0옴 추가
6. "USB+5V" Silk 부분 옆에 Font 크기대로 수정
7. C46과 R35 실크 변경

▷ DIGCOM XA(Xilinx-Artix) Board V1.0



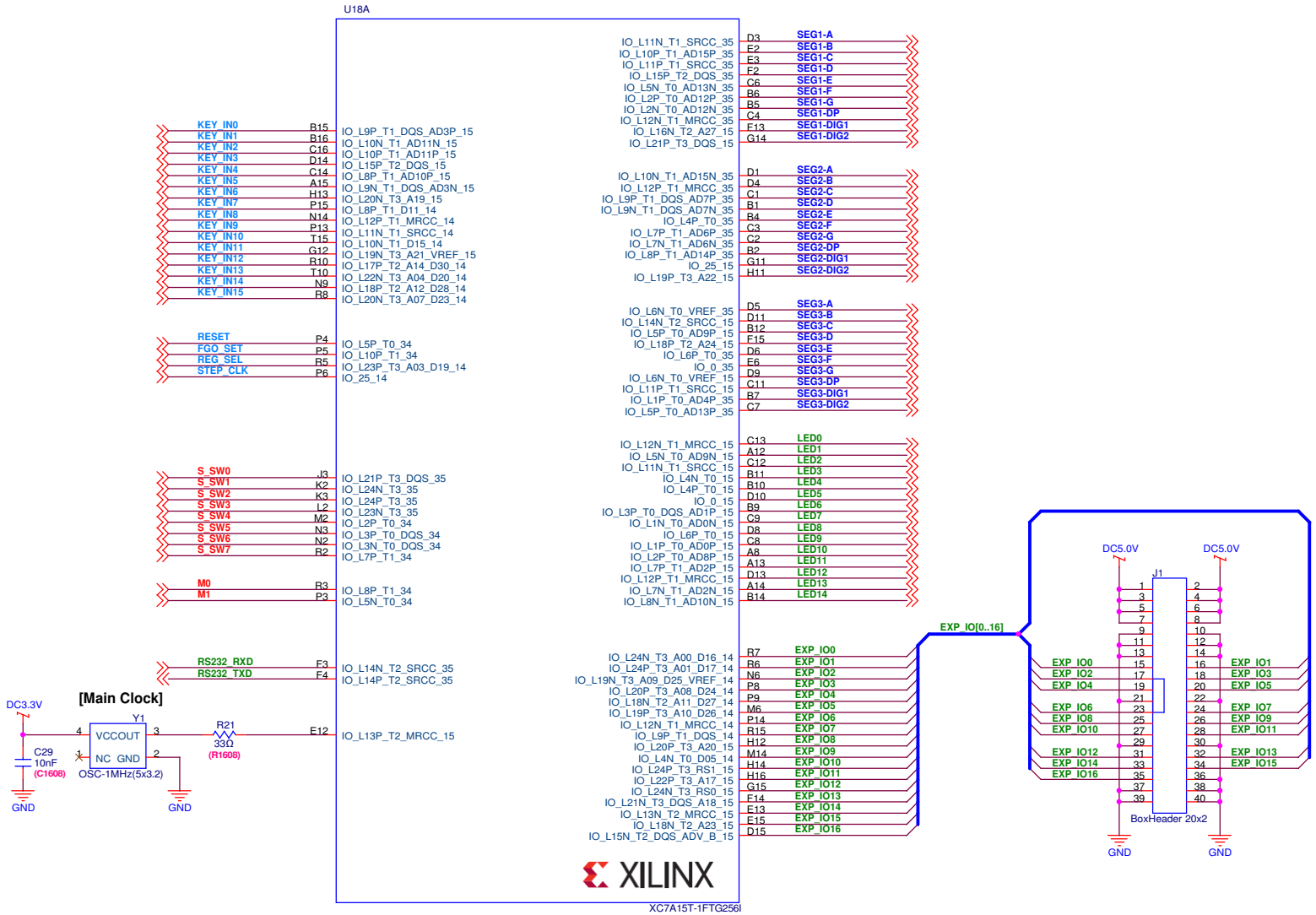
Title	▷ DIGCOM XA(Xilinx-Artix) Board V1.0	
Size A3	Document Number: Push Key and LED, 7-Segment Interface	Rev 1.0
Date: Monday, March 20, 2017	Sheet 1 of 5	

▷ DIGCOM XA(Xilinx-Artix) Board V1.0



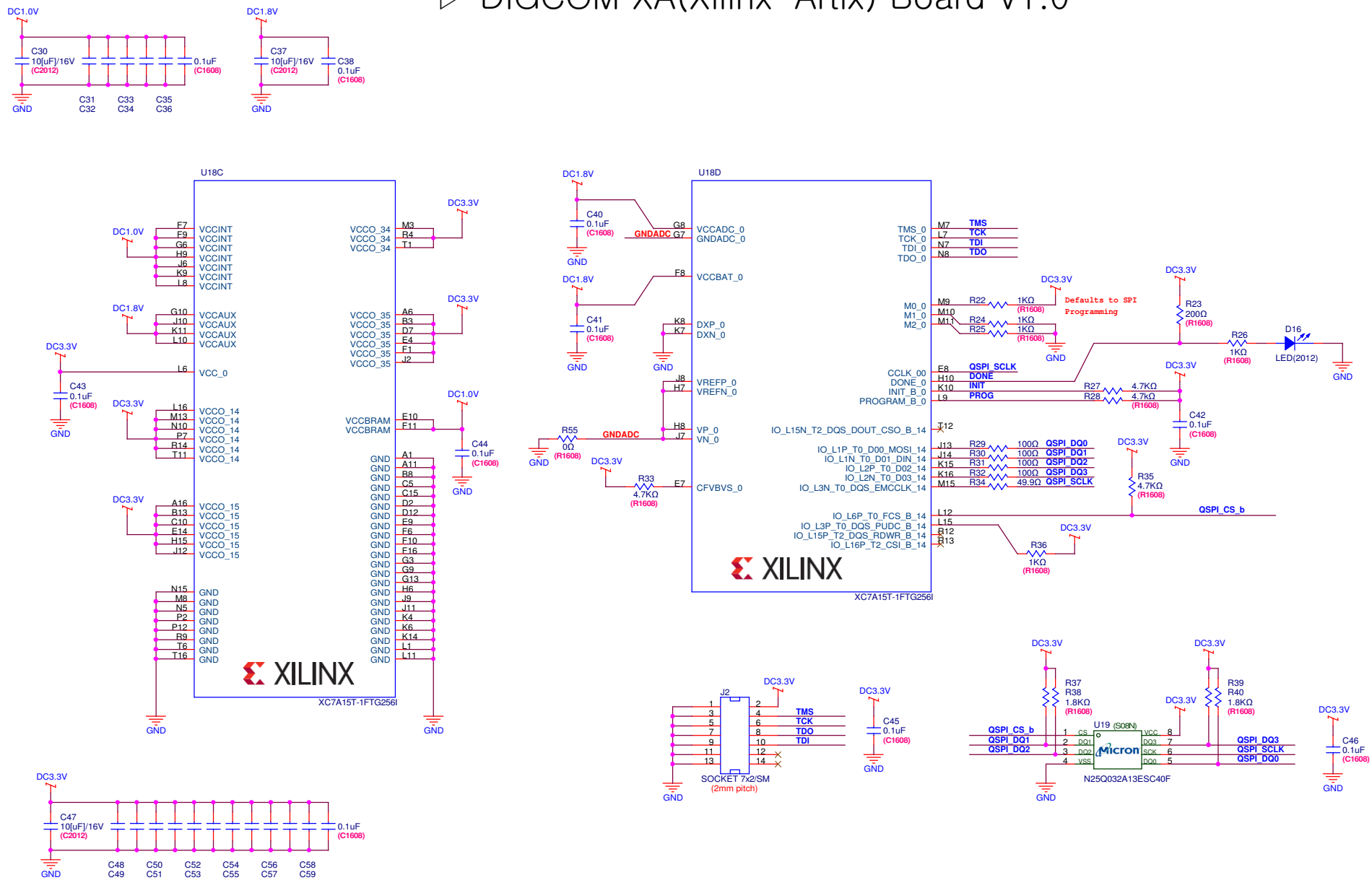
Title	▷ DIGCOM XA(Xilinx-Artix) Board V1.0	
Size A3	Document Number Slide Switch Interface	Rev 1.0
Date: Thursday, March 16, 2017	Sheet 2 of 5	

▷ DIGCOM XA(Xilinx-Artix) Board V1.0



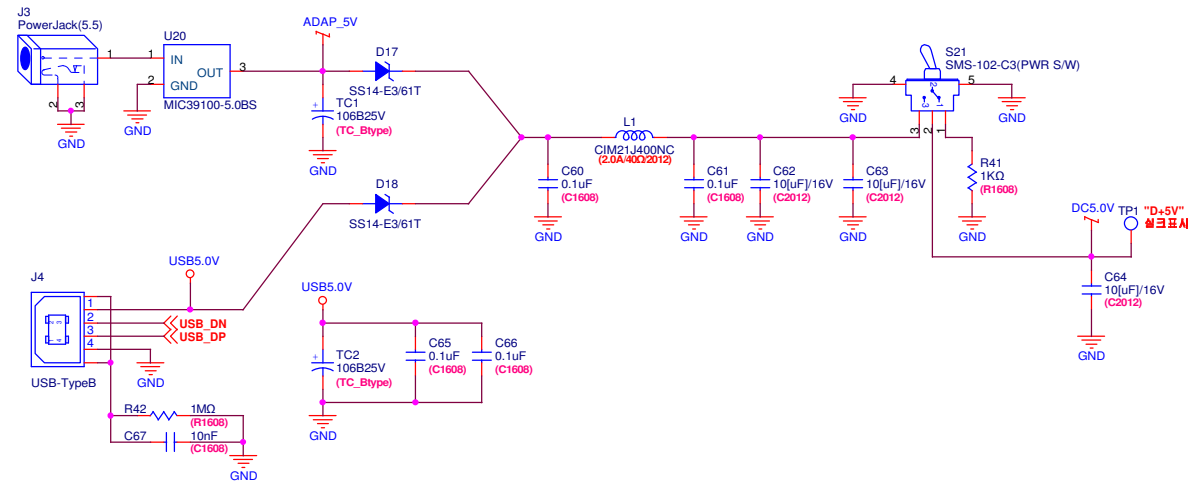
Title	▷ DIGCOM XA(Xilinx-Artix) Board V1.0	
Size A3	Document Number FPGA I/O Interface	Rev 1.0
Date: Thursday, March 16, 2017	Sheet 3 of 5	

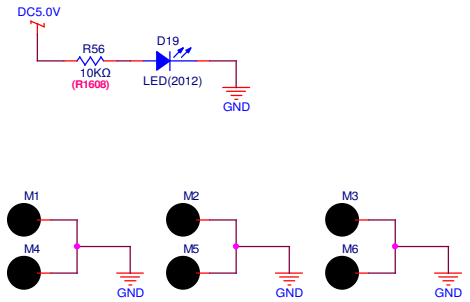
▷ DIGCOM XA(Xilinx-Artix) Board V1.0



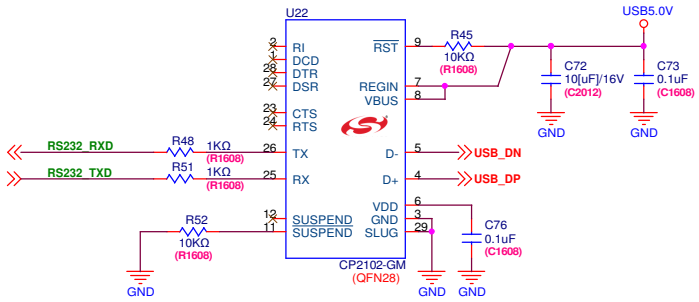
Title	▷ DIGCOM XA(Xilinx-Artix) Board V1.0	
Size A3	Document Number FPGA JTAG and Core Interface	Rev 1.0
Date: Monday, March 20, 2017	Sheet 4 of 5	

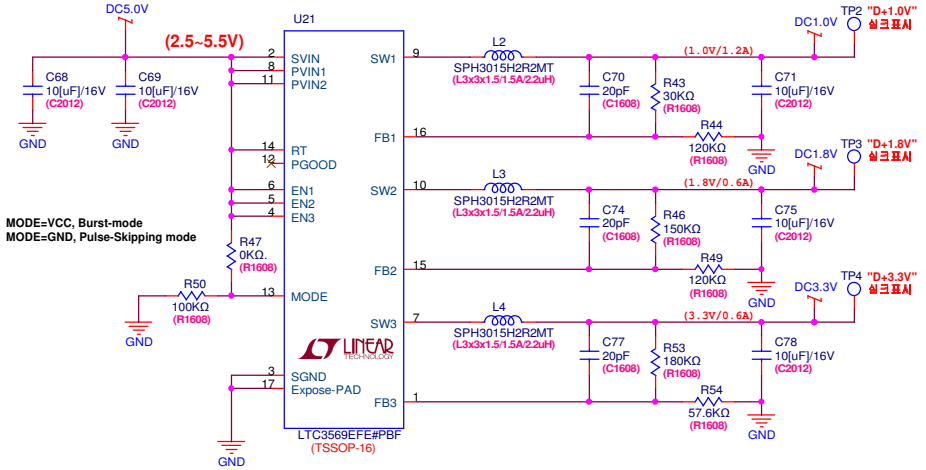
▷ DIGCOM XA(Xilinx-Artix) Board V1.0





■ USB to UART Bridge





Title	▷ DIGCOM XA(Xilinx-Artix) Board V1.0	
Size A3	Document Number Power Interface	Rev 1.0
Date: Monday, March 20, 2017	Sheet 5 of 5	